Journal of Computer Science 3 (9): 765-772, 2007
ISSN 1549-3636

Automatic Calibration of Frequency Compensation System in Computer-Controlled Patch-Clamp Amplifier

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Abstract: Computer-controlled patch-clamp amplifier is a digitally controlled analog device used to record the cellular ion channel currents in electrophysiology research. The inherent bandwidth and performance of the headstage is limited by the stray capacitance and distributed capacitance across the feedback resistors. In order to effectively improve the performance of the headstage, the paper advanced a simplified automatic calibration method of frequency compensation system in resistor-feedback patch-clamp amplifier. The dynamic model of headstage was approximate as a two poles and one zero system in the transfer function by experience and test results, so the dynamic characteristics of the headstage were obtained employing least squares parameter estimation algorithm. Further more, the compensation parameter of high frequency booster can be estimated by the time constant of main pole of headstage. And automatic adjustment of the parameters in transient response correction stage was performed as a least squares fitting problem. The software routine running on the host computer conducted all operations of frequency compensation. Experimental results demonstrate that the simplified automatic calibration method can substantially extend the bandwidth and minimize step response error of headstage.

Key words: Patch-clamp, least-squares parameter estimation, high frequency compensation, transient response correction

INTRODUCTION

Patch-clamp amplifier can be used to record the single-channel and whole cell currents in electrophysiology research[1,2]. It is fundamentally a sensitive current- to-voltage converter, converting small (picoampere to nanoampere) cellular ion channels currents into voltage signals that can be observed with oscilloscope or sampled by data acquisition (DAQ)[3,4].

Compared to the conventional patch-clamp amplifier, computer-controlled patch-clamp system implemented digital control of all functions and adjustable parameters in the amplifier circuitry through the software running on the host computer. Further more, mode switching, capacitive transient cancellation, series resistance compensation and a number of other operations are automated. The digital control of the analog circuitry is mainly performed through multiplying digital-to-analog converters (mDACs) and analog switch devices. In the amplifier circuitry, mDACs perform as variable resistors replacing potentiometers and analog switch devices replace conventional ones[5,6].

Parasitic capacitance across the feedback resistors in the headstage introduces non-ideal frequency characteristics that must be compensated for and frequency compensation system was developed to do it. In conventional patch-clamp amplifier, the potentiometers in the frequency compensation stage were adjusted manually to correct the frequency response, which is a time-consuming process. So Sigworth had advanced an automatic calibration method to perform the adjustment of the frequency compensation system[7]. Here we used a simplified automatic calibration method to perform adjustment of the frequency compensation system on the basis of the approximate dynamic model of headstage and Sigworth's work.

MATERIALS AND METHODS

System overview: The new computer-controlled patch-clamp system PC3 was researched and designed by

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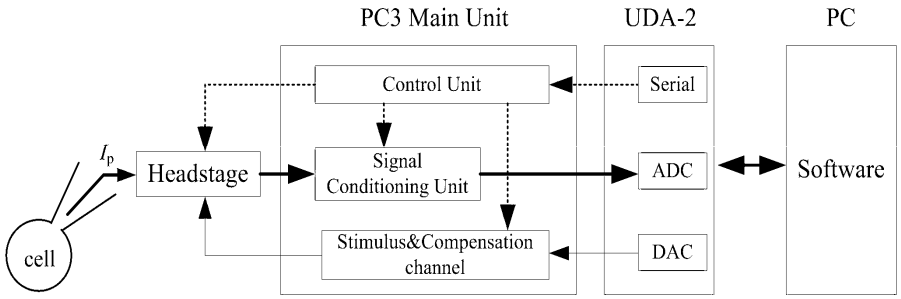

Fig. 1: Diagram of computer-controlled patch clamp system

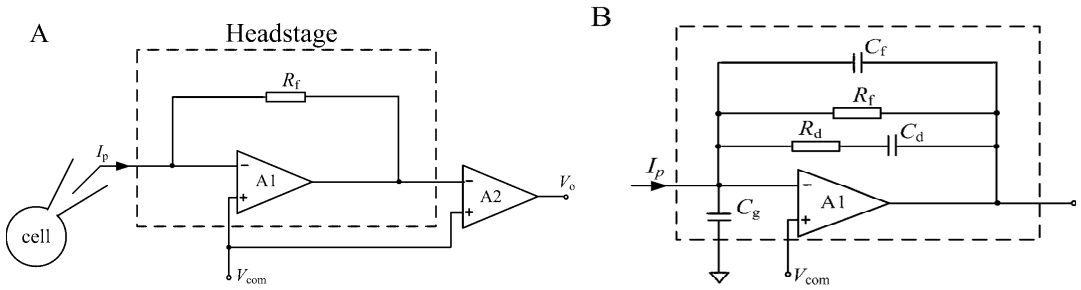

Fig. 2: Resistor-feedback headstage of patch clamp amplifier. (A) Principle of resistor-feedback patch clamp amplifier. Operation amplifier A1 is configured as a current-to-voltage converter. Differential amplifier A2 subtracts V_{cmd} from the output of A1 to generate a voltage that is purely proportional to the voltage across R_f. (B) The dynamic characteristic model of resistive headstage

institute of biophysics and biochemistry of Huazhong University of science and technology. The system consists of a headstage amplifier, patch-clamp amplifier main unit, data acquisition interface and personal computer (Fig. 1). The patch-clamp amplifier contains no processor in itself, but relies on data acquisition and control software running on the host computer, which provides the initialization, control, calibration and testing of its analog functions.

For the reason of the asynchronism of the A/D and D/A on common DAQs, we have designed a novel USB2.0-based DAQ, in which four 12-bit DAC channels, eight 333 kHz 12-bit ADC channels and a serial interface are provided. Two DAC channels are dedicated to providing stimulus voltages and test signals and two ADC channels are dedicated to sampling the current monitor signals and the measure points' output signals from the internal multiplexer. The reminding DAC and ADC channels are left free for other uses. The serial interface in DAQ is designed to transfer the control codes from the software running on the host computer to the control and interface unit in PC3. Then control and interface unit decodes the serial data and controls the analog switches and mDACs by the programmable logic device. The stimulus and compensation stage of patch-clamp amplifier scales the command voltages and injects the currents used for the capacitance transient cancellation and series resistances compensation. The signal-conditioning unit (including frequency compensation system) reconstructs the output of headstage and formats the signal into the form required by DAQ.

To allow for automatic calibration and testing of the circuitry of the patch-clamp amplifier, 16 measure points are added into the circuitry. All measure points are brought through an internal multiplexer to the dedicated ADC channel. Test signals from the dedicated DAC were injected into the circuitry channel at the four test points and analog switches set the point for the injection of test signal.

Dynamic model of headstage: The headstage of patch-clamp amplifier is a high-sensitive current-to-voltage converter. The simple way to measure small currents is to monitor the voltage drop across a large resistor. Fig. 2A shows the circuits of a resistive headstage. The operation amplifier A1 is configured as a current-to-voltage converter. A1 varies output to keep the pipette potential at V_{com}. Differential amplifier A2 subtracts V_{cmd} from the output of A1 to generate a voltage that is

purely proportional to the voltage across R_f[3]. Thereby, the desired current is obtained.

In order to increase the sensitivity, the value of feedback resistors is very large commonly. The PC3 headstages uses the resistors of 500 MΩ (for whole cell mode) and 50 GΩ (for single channel mode). Commercial resistors in this range have some inevitable parasitic capacitance, including the stray capacitance C_f, distributed capacitance C_d and input capacitance C_g (Fig. 2B).

- The inherent bandwidth of a feedback resistor is limited by the stray capacitance C_f. For example, the 50 GΩ resistors with 0.1 pF (picofarad) stray capacitance has a time constant of 5 ms, corresponding to a bandwidth of about 32 Hz. The time resolution is very low, which is unacceptable for measuring the ionic currents
- The distributed capacitance C_d in the high-value resistors makes the headstage model more complex, because R_f cannot be considered as an ideal capacitor C_f in parallel with an ideal resistor. C_d and R_d will introduce a differential into the circuits
- When a step voltage command is applied on the pipette, the current required to charge the input capacitance C_g will easily exceed the maximum range that can be passed by R_f. As a result, the patch clamp amplifier will be saturated. In order to compensate the charging current through C_g, a special circuit (fast capacitance compensation circuits in stimulus and compensation channel of PC3) was developed to inject the required charging current. The circuit and method of C_g compensation exceeds the scope of this paper and will not be discussed here

In conclusion, the influence of parasitic capacitance across the high-value resistor can't be ignored. The dynamic model of headstage can be approximated to two poles and single zero in transfer function by experience and test. The response characteristics of the headstage are described by a transfer function Z(s), which can be used to give the response V(s) at the output of headstage for any input current I(s)

$$Z(s) = \frac{V(s)}{I(s)} \approx R_f \frac{\tau_z s + 1}{(\tau_m s + 1)(\tau_p s + 1)} \quad (1)$$

Where $s = j\omega$, R_f is the feedback resistor, τ_0, τ_m and τ_p are the equivalent time constant of main pole, sec pole and zero in the headstage, respectively. τ_z and τ_p approximately represent characteristic in high frequency.

When R_f is 500 MΩ, τ_m is about twenty times greater than τ_z and τ_p by experience, so the model can be simplified as a first order delay component[8]. Otherwise, τ_m, τ_z and τ_p were in the same range (several ms) when R_f is set as 50 GΩ. Thus, the compensation of headstage that R_f is 50 GΩ is more difficult than that R_f is set as 500 MΩ. So, we here just discuss the automatic calibration method of the compensation system for the headstage that R_f set as 50 GΩ in detailed.

AUTOMATIC CALIBRATION METHODS

Compensation methods: The headstage consists of a low-noise operational amplifier, analog switches, feedback resistors of 50 GΩ, 500 MΩ and current-injection capacitors of 1 pF and 10 pF (Fig. 3). Because the headstage is physically small, the necessary gain and frequency compensation adjustments are implemented in the main unit of patch-clamp amplifier. Diagram of frequency compensation for the headstage was summarized in Fig. 3.

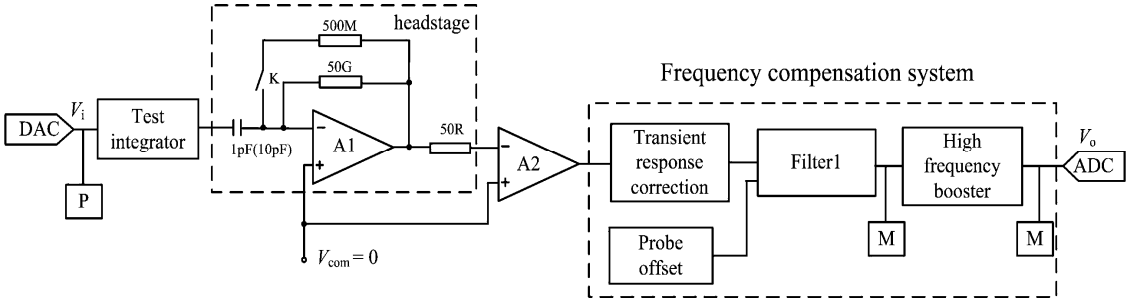

Fig. 3: Block diagram of calibration of frequency compensation system of patch-clamp amplifier

The test signal from the dedicated test DAC channel is injected into the circuit at the test point (P in Fig. 3). An auto-zeroing test integrator is provided to allow currents to be injected through injection capacitors into the headstage to test the frequency response of the headstage. Then current-monitor signals of the headstage pass through transient response correction stage (correcting for distributed capacitances across the feedback resistors), filter1 (reducing the high-frequency noise) and high frequency booster (correcting the main pole introduced by the stray capacitance across the feedback resistors). To allow for automatic calibration of frequency compensation system, two measure points (M in Fig. 3) are intercalated for monitoring the output of transient response correction stage and high frequency booster.

Estimate dynamic model of headstage: Eq.1 can be rewritten as

$$Z(s) = \frac{V(s)}{I(s)} \approx R_f \frac{b_1 s + b_0}{a_2 s^2 + a_1 s + 1} \tag{2}$$

Where $s = j\omega$, R_f is the feedback resistor.
Because the headstage is approximate to a two-pole system, the parameters of elements b_0, b_1, a_1, a_2 of Eq. 2 can be determined by the least squares parameter estimation algorithm[9], as shown in Eq. 3.

$$\begin{bmatrix} \lambda_0 & 0 & T_1 & S_2 \\ 0 & \lambda_2 & -S_2 & T_3 \\ T_1 & -S_2 & U_2 & 0 \\ S_2 & T_3 & 0 & U_4 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} S_0 \\ T_1 \\ 0 \\ U_2 \end{bmatrix} \tag{3}$$

Where $\lambda_i = \sum_k \omega_k^i$, $S_i = \sum_k \omega_k^i P(\omega_k)$, $T_i = \sum_k \omega_k^i Q(\omega_k)$, $U_i = \sum_k \omega_k^i [P^2(\omega_k) + Q^2(\omega_k)]$, $P(\omega_k) = \mathrm{Re}[Z(j\omega)]$, $Q(\omega_k) = \mathrm{Im}[Z(j\omega)]$, k = 1, 2, 3…n.

The frequency response of the headstage was tested using swept frequency sine waveform stimulus signals. Because the bandwidth of 50 GΩ is about 20 Hz, so we set the frequency of test sine signals as 10 Hz to 70 Hz with 5 Hz step. The amplitude was 2 V peak-to-peak. The stimulus signals pass through auto-zeroing test integrator and 1 pF current-injection capacitor and apply at the input of the headstage. The calibrated currents are 200 pA peak to peak. A procedure creates and analyzes the responses and stimulus signals using FFT. Forty cycles waveform of each frequency were delivered; the sec half of responses are averaged and the results are transformed to obtain the gain and phase at half cycle points. Then b_0, b_1, a_1 and a_2 can be obtained using the gain and the phase of all frequency test points and Eq. 3.

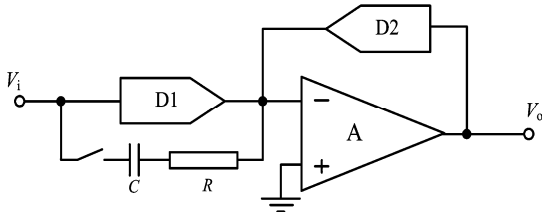

Fig. 4: High frequency compensation stage D1 and D2 act as a variable conductance. The C is 330 nF and R is 50 Ω when the stage was set for compensating the 50 GΩ headstage resistor

High frequency boost: Two 12-bit mDACs D1, D2 (AD7564, Analog Devices) are used to set both gain and the time constant in the high frequency booster[5,6], as shown in Fig. 4. The transfer function of high frequency booster is

$$H(s) = -\frac{D_2}{D_1} \cdot \frac{(D_1 + R)Cs + 1}{RCs + 1} \tag{4}$$

where D_1, D_2 are the equivalent resistances of mDAC D1 and D2 respectively.

D1 acts as a variable conductance to set the time constant of zero. D2 sets the overall gain by acting as the feedback resistor. For the equivalent resistance of D1 is far larger than R, the time constant of zero τ_0 in high frequency booster is approximate to D_1C. The time constant of new pole of the stage is RC and far less than τ_0. So, the bandwidth of new pole of high frequency stage is above 10 kHz, which is enough for measuring ionic currents.

The time constant of the main pole τ_m of headstage can be cancelled exactly when $\tau_0 = \tau_m$. Nevertheless, τ_0 is set to be equal to or a little larger than the calculated parameter τ_m to ensure the enough compensation for the headstage. The residual error of step response after compensation is

$$e(t) = (\frac{\tau_0}{\tau_m} - 1)\exp(-\frac{t}{\tau_m}) \tag{5}$$

Transient response correction: After enough high frequency compensation, the step response exhibited an

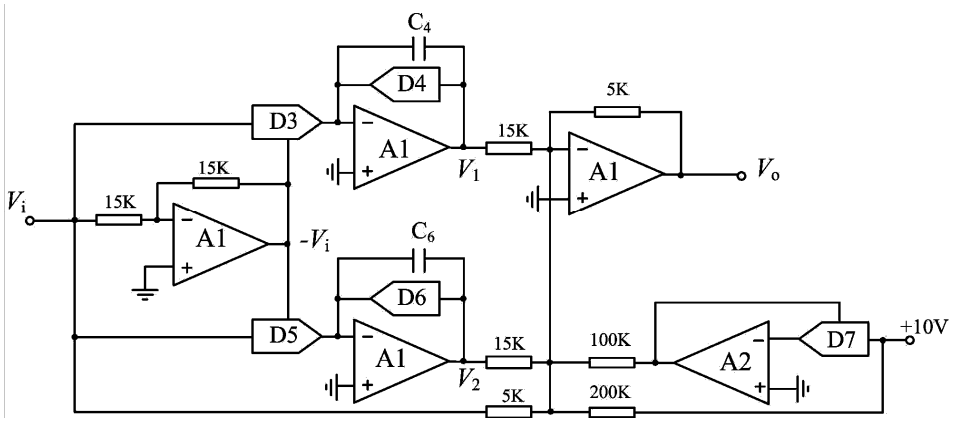

Fig. 5: Transient response correction stage circuitry

overshoot that arises by the distributed capacitor C_d. The overshoot can be removed by the transient response correction stage as shown in Fig. 5, which consists of parallel first-order filter components. The transfer functions of dual first-order filter are

$$H_1(s)=\frac{V_1(s)}{V_i(s)}=\frac{a_1}{\tau_1 s+1}$$
$$H_2(s)=\frac{V_2(s)}{V_i(s)}=\frac{a_2}{\tau_2 s+1} \quad (6)$$

where τ_1 and τ_2 are the time constant of the filter, a_1, a_2 are the amplitudes of filter components.

The overall transfer function of transient response correction can be written as

$$H(s)=1+\frac{k_1}{\tau_1 s+1}+\frac{k_2}{\tau_2 s+1} \quad (7)$$

where $k_1 = -0.34\ a_1$, $k_2 = -0.34\ a_2$.

The adjustment of the four parameters in Eq. 7 is performed as a least squares fitting problem. The two amplitude parameters have linear effects and optimum values can be computed using least-squares algorithm. Otherwise, the two time constant parameters have non-linear effects and finding the optimum values was a difficult problem. The best approach to finding the optimum set of these two non-linear parameters was a search of their domains[7]. At each point in a grid of 20*20 values for τ_1 and τ_2, a_1 and a_2 were determined and the residual error was predicted respectively.

The difference between step response of headstage after transient response correction and high frequency boosted and the idea value is

$$E=\sum_n [f_0(n)+k_1 f_1(n)+k_2 f_2(n)-M(1+k_1+k_2)]^2 \quad (8)$$

where $f_0(n)$ is the step response of system when $k_1 = k_2 = 0$, M is the steady state value of f_0; $f_1(n)$ is the step responses of system when $k_1 = 1$, $k_2 = 0$; $f_2(n)$ is the step responses of system when $k_1 = 0$, $k_2 = 1$.

When the value of τ_1 and τ_2 is initialized, the optimization value of k_1, k_2 can be obtained when

$$\frac{\partial E}{\partial k_1}=0, \frac{\partial E}{\partial k_2}=0 \quad (9)$$

so k_1, k_2 are given by

$$k_1=\frac{KV-QU}{PQ-K^2}, k_2=\frac{KU-PV}{PQ-K^2} \quad (10)$$

Where $P=\sum_n [f_1(n)-M]^2$, $Q=\sum_n [f_2(n)-M]^2$, $U=\sum_n [f(n)-M][f_1(n)-M]$, $V=\sum_n [f(n)-M][f_2(n)-M]$, $K=\sum_n [f_1(n)-M][f_2(n)-M]$.

In order to speed the search, actual step responses of the system were only measured under the condition that k_1 and k_2 were set to zero at first; the effect of non-zero amplitudes of these components was then computed numerically to quickly evaluates the step response. $f_1(n)$, $f_2(n)$ can be computed numerically by first-order recursive filter method.

When the transfer function of first-order filter is $H(s) = \frac{m_0}{s + m_1}$, the output $f(n)$ can be numerically arithmetic estimates by the following[10]:

$$f(n+1) \approx e^{-m_1 T} f(n) + \frac{m_0}{m_1}(1 - e^{-m_1 T})u(n)$$

$$f(0) = u(0) \tag{11}$$

where u(0) is the input of filter; T is the sample interval.

Several candidates for the optimum values of the amplitude parameters and time constant parameters were obtained as the grid point yielding the smallest error. Every team of parameters is loaded into the corresponding mDACs and the response at the output of high frequency booster was measured when the scaled square-wave current injected. The best optimization of all four parameters was obtained by minimizing of the measured peak error after every team parameters were used to set mDACs in the circuits.

Gain scaling: D2 is used to set the gain of the frequency compensation system (Fig. 3). At final step, we adjusted D2 to scale the gain of the headstage. The scaled gain at the output of high frequency booster stage is 0.5 mV/pA (500 MΩ) or 50 mV/pA (50 GΩ). Gain scaling used an iterative search routine that based on a linear approximation (Newton-Raphson) method.

After high frequency compensation, transient response correction and gain scaling, all the parameters were stored in the file on the host computer and then used by the patch-clamp experimental software.

RESULTS

The method described in Estimate dynamic model of headstage was used to test the frequency characteristics of the headstage. The frequency response of headstage was shown in Fig. 6 and the dynamic parameters were obtained accordingly. The main time constant is about 8.88 ms, so the bandwidth of the headstage is about 20 Hz, which is too narrow for measuring ion channel currents. As shown in Fig. 7A, the high frequency portion of signal was attenuated when the step signal passed through the headstage. The test signal injected at the input of headstage had been scaled to 200 pA(-100.0 pA to 100.0 pA) by the auto-zeroing test integrator and 1 pF injection capacitor. And the test signal frequency was 25 Hz.

In order to completely compensate the main pole of the headstage, the time constant τ_0 of zero in high-frequency correction stage is a little larger than the estimated time constant of main pole of headstage. And the choice of τ_0 should ensure that the steady state of the step response is very flat and the overshot is as little as possible. As a consequence, τ_0 is set to be 8.90 ms. For the C for compensating 50 GΩ is 330 nF, the effective resistance of mDAC (D1 in Fig. 4) should be about 27 kΩ. D2 sets the overall gain by acting as the feedback element, so it should be initialized to a fixed value (2500 in our system) at first and rescaled at the final step.

The step response of system after high-frequency compensation was shown as Fig. 7B. Step response exhibited a serious overshot which was produced by the zero of headstage. The procedure estimated τ_1, τ_2 and a_1, a_2 using the least squares fitting method described in Transient response correction. The optimum value of τ_1, τ_2 is estimated as 0.45 ms and 3.11 ms and the corresponding values of a_1, a_2 as 0.15 and 0.69, respectively. The parameters are loaded into the appropriate mDACs (D1, D2, D3 and D4 in Fig. 5) and the responding signal was acquired by DAQ (shown in Fig. 7C).

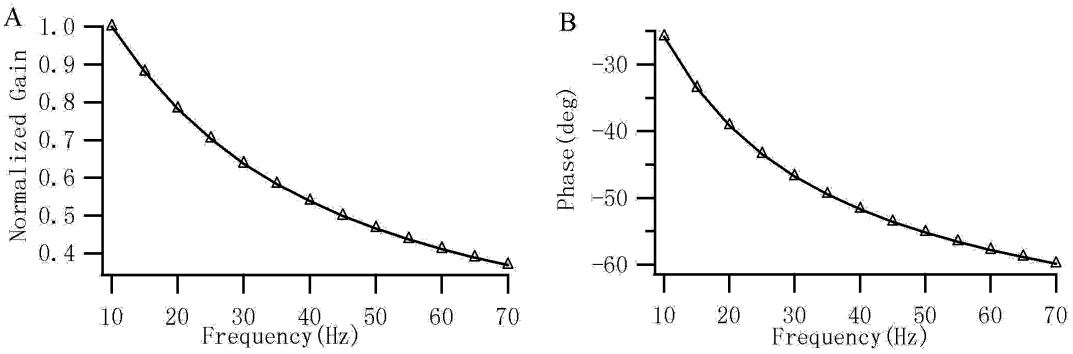

Fig. 6: Frequency-response of headstage when the feedback resistor is set to be 50 GΩ. (A) The relationship between normalized gain and frequency of input signals. (B) The relationship between phase and frequency of input signals

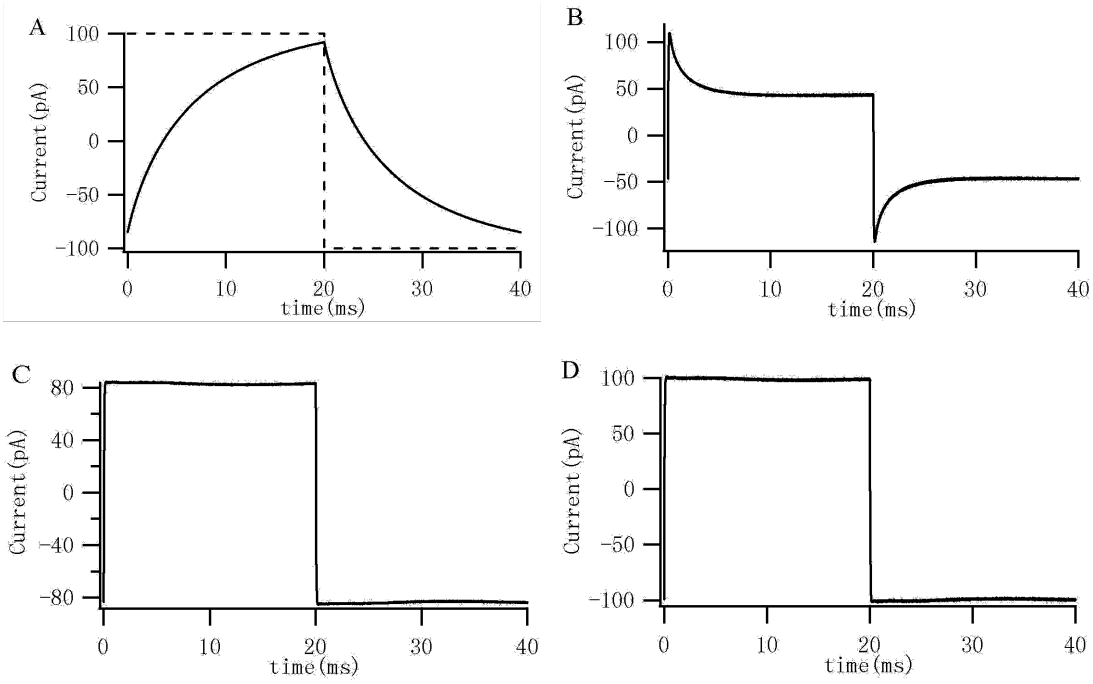

Fig. 7: Results of frequency compensation. (A) Step response of the headstage. The real line is step response; the dashed is stimulus signal. (B) The step response after high-frequency correction. (C) The step response after transient correction. D() The step response after gain scaled of the headstage. The stimulus signal of each step was a scaled 25 Hz, 200 pA(-100.0 pA to 100.0 pA) step current signal as shown in A

At the final step, we adjusted the code of D2 in Fig. 4 to ensure that the actual gain of the system is same to the designed value. The designed gain of the headstage is 50 mV/pA when a 50 GΩ feedback resistor was used. The output of high-frequency booster is 10 V (peak to peak) after gain scaling, so the equivalent of current is 200 pA (-100 pA to 100 pA) (Fig. 7D).

We found that the simplified calibration method of the frequency compensation system can remarkably accelerate the system response (Fig. 7). The result data demonstrate that the extended bandwidth of headstage can reach above 6 kHz, which is about 300 times larger than the original value before compensation and is enough for measuring physiological signals. The residual error is less than 2% after transient response correction. Similar results were obtained in the experiments of replacing other two headstages.

DISCUSSION

The automatic calibration routine of frequency compensation system is of great interest for both manufacturer and users. First, the manual adjustment of frequency correction stage circuits in the conventional patch-clamp amplifier is difficult and time-consuming. But for the new type amplifier, the manufacturer just needs perform the software routine to calibrate the frequency compensation system and save the results in host computer. The whole process for each of the two ranges takes about 3 min on personal computer.

Second, compensation results of the headstage are dependent on dynamic characteristics and manufacture crafts of the feedback resistors used. Since the noise level and dynamic characteristic cannot be predicted, various brands and several of resistors must be tested until the best one is founded in the conventional patch-clamp amplifier, which is also a time-consuming process. The automatic calibration method makes the choice of resistors and adjustment of frequency compensation system much more efficient and simple than before.

Third, the necessary gain and frequency compensation adjustments must be made whenever the headstage is exchanged. In conventional patch-clamp amplifier, setups of frequency compensation system circuits were unchangeable for users after calibration and the patch-clamp main unit and headstage must send to the manufacturer for recalibrating it. The calibration results of the novel patch-clamp amplifier are saved in the computer, so the automatic calibration routine is

valuable both for manufacture and user to recalibrated the main unit and save the results in host computer after replacing the headstage.

CONCLUSION

The automatic calibration of the frequency response of headstage is the most demanding portion of computer-controlled patch-clamp amplifier. Experimental results of demonstrate that the frequency compensation system calibrated by our automatic calibration method can reconstruct the signals pass through the headstage accurately and effectively.

The implement of complete digital control of patch-clamp amplifier has resulted in an instrument having some advantages. It's more convenient and easy to operation by mouse and keyboard than the knobs and switches of the conventional patch clamp amplifier. Further more, the software routines running on the computer can perform some functions to realize the automatic calibration, testing and adjustment and the routines perform their functions more quickly than the corresponding manual adjustment.

ACKNOWLEDGEMENT

This work was supported by National Science Foundation of China Grant 30327001.

REFERENCES

1. Neher, E. and B. Sakmann, 1976. Single-channel currents recorded from membrane of denervated frog muscle fibres. Nature, 260: 799-801.
2. Hamill, O.P., A. Marty and E. Neher *et al*., 1981. Improved patch-clamp techniques for high-resolution current recording from cells and cell-free membrane patches. Pflfigers Arch., 391: 85-100.
3. Rivka, S.G., 1993. Instrumentation for measuring bioelectric signals from cells. In: The Axon Guide for Electrophysiology and Biophysics Techniques (eds Rivka, S.G.). Axon Instruments Inc., Foster City, CA, pp: 25-80.
4. Sigworth, F.J., 1994. Electronic design of the patch clamp. In: Single Channel Recording(eds Sakmann, B., Neher, E., 2nd edition). Plenum, New York, pp: 95-127.
5. Sigworth, F.J., 1995. Design of the EPC9, a computer-controlled patch-clamp amplifier. 1. Hardware, J. Neurosci. Methods, 56: 195-202.
6. Alzaher, H. and M. Ismail, 2000. Digitally tuned analog integrated filters using the R-2R ladder. Electronics, Circuits and Systems (ICECS), pp: 383-385.
7. Sigworth, F.J., H. Affilter and E. Neher, 1995. Design of the EPC9, a computer- controlled patch-clamp amplifier. 2. Software, J. Neurosci. Methods, 56: 203-215.
8. Hu, G., Q.H. Zhu and A.L. Qu, 2005. Designing a signal conditioning system with software calibration for resistor-feedback patch clamp amplifier. The 27th Annual International Conference of the IEEE-EMBC, pp: 6729-6732.
9. Ljung, L., 1999. System Identification: Theory for the User. Prentice Hall.
10. D'Azzo, J., C. Houpis and S. Sheldon, 2003. Linear Control System Analysis and Design With Matlab, Marcel Dekker Inc., New York, pp: 88-106.