FPGA IMPLEMENTATION AND ANALYSIS OF IMPULSE NOISE REDUCTION IN IMAGES

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ABSTRACT

The images are affected by random valued impulse noises during the image capturing and processing stages. In this study, an efficient, high performance and low hardware utilized impulse noise reduction algorithm is presented. This methodology determines the optimum direction pixels through the estimation of standard deviation. The edges in the images are preserved during the process of impulse noise detection and removal stage. The hardware architecture for this design is proposed and its performance is analyzed with different FPGA Processors in terms of slices, LUTs and power consumption. The proposed hardware architecture consumes 1728 gates and power consumption of 159.95 mW. The main motivation behind this research is to design low power impulse noise detection architecture and its real time implementations.

Keywords: Impulse Noise Reduction, Optimal Detector, Power Consumption, Edge Detection, Image Quality

1. INTRODUCTION

In recent eras of image processing, during image acquisition and transfer, images are often corrupted by impulse noise which is a major factor affecting the contents of a digital image. Mostly the impulse noise occurs due to electromagnetic interference, synchronization errors in digital recording and problems within communication devices. Impulse noise deforms the image pixels while replacing the original pixel values by fixed values or random values. In fixed-value impulse noise, the gray value is a fixed value, i.e., either 0 or 255 (example: Salt and pepper noise). In random-value impulse noise, gray value is a value between [0, 255]. The random valued impulse noise has randomly distributed noise pixels and hence requires more effort to be removed.

Digital signal processing frequently involves some method for noise reduction over an image. The median filter is a non-linear digital filter, which is most popularly used to remove impulse noises. Many popular algorithms were presented which eliminates impulse noises present and maintains only the fine details of the image. But, median filter preserves the edges of the image by uniform modification of the noise affected pixels and the noise-free pixels. Also, the conventional filters work better only over images affected with low noise ratios and is very poor when the noise ratio reaches above 40%. Recent statistic filter finds the relative difference in detecting more edge pixels, by implementation of statistic of rank-ordered absolute difference over the relative difference image and not over the noise corrupted image.

Our denoising algorithm performs spatial processing and preserves the image details as an advantage to other filtering techniques. Another advantage is that use of adaptive mean filtering does not affect the edges or other small structures in the image. The method is more efficient for the images with very high noise ratio.

The Centre Weighted Median (CWM) filter is a weighted median filter which gives more weight to the

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centre value of each window. This filter can preserve image details by suppressing additive white Gaussian noise or impulse noise. As this filter gives more weight to the central value of a window, it is easier to design and implement than the weighted median filters.

There are several researches regarding VLSI implementation of low complexity optimal detection algorithms. The impulse noise reduction technique by finding the optimal direction is implemented as an efficient VLSI architecture design with reduced complexity. Our design uses a low-cost edge detection technique and efficient pipeline architecture to achieve high performance at low cost.

2. RELATED WORKS

A two-stage iterative method was proposed for removing random valued impulse noise. In the first stage, an adaptive centre-weighted median filter is used for identifying pixels which are likely to be corrupted by noise. In the second stage, these noise candidates are restored using a detail-preserving regularization method which allows edges and noise-free pixels to be preserved. These two phases are applied alternatively. Simulation results proved their method to be considerably better than other methods using only non-linear filters or regularization.

Chen *et al.* (2010) has proposed low cost VLSI implementation for efficient removal of impulse noise. Their extensive experimental results show that the proposed technique preserves the edge features and obtains excellent performances in terms of quantitative evaluation and visual quality. Smolka (2012) proposed a new approach for removing impulse noise in color images. The design used the vector median filter and is based on the weighting of the dissimilarity measures between pixels contained in the local filtering window. The weights assigned to each color sample are decreasing functions of their ranks in an ordered sequence, while the ordering is based on the distance between a given pixel and its neighbours. Extensive experiments proved that their filtering design efficiently removed the impulse noise in color images while enhancing their edges. This unique feature can be utilized in any application in which noise removal combined with edge enhancement is needed.

Luisier *et al.* (2011) has proposed an efficient image denoising in Mixed Poisson-Gaussian Noise. Their design possesses low computational complexity and two line memory buffers with very low hardware cost. Synthesis results showed that the proposed design yields a processing rate of about 167 M samples/second by using TSMC 0.18 µm technology. Boulanger *et al.* (2010) achieved low PSNR values and did not concentrate on the edges while denoising process. Rezvanian *et al.* (2008) has proposed two-pass method to impulse noise reduction from digital images based on neural networks. The algorithm was developed based on two schemes, i.e., (1) switching scheme-an impulse detection algorithm is used before filtering, thus only a proportion of all the pixels will be filtered and (2) progressive methods-both the impulse detection and the noise filtering procedures are progressively applied through several iterations. The simulation results proved that the algorithm was effective for the cases where the images are very highly corrupted. Yu *et al.* (2008) has developed an efficient procedure for removing random-valued impulse noise in images. It provided very moderate PSNR as image quality measurement parameter. Al-Araji *et al.* (2007) has developed impulsive noise reduction techniques based on rate of occurrence estimation. Lien *et al.* (2013) has proposed an efficient denoising architecture for removal of impulse noise in images. Chapter 3 propose an efficient impulse noise filtering algorithm and chapter 4 discusses the results achieved with various state of arts.

3. PROPOSED OPTIMAL DETECTOR NOISE FILTERING ALGORITHM

The proposed noise removal technique uses an innovative algorithm which finds the optimal direction which is used as a measure to detect whether the currently processed pixel is noisy or noise-free. The edge pixels are detected more if the optimal direction of the edge is found out accurately.

3.1. Algorithm Design

The algorithm design includes two steps, dividing the filtering window into four directions and finding of the optimal direction. The optimal direction is the direction with more identical pixels.

At the first step, the image which is to be denoised is first split into m×n pixel blocks as shown in **Fig. 1**. These blocks should not be overlapped with each other. In our research, we split the noised image of size 36×36 into 16 numbers of 16×16 sub-block. Each sub-block is of size 16×16.

Next, the first sub-block (of size 9×9) is divided into four Orthogonal Directional Patterns (ODP) as shown in **Fig. 2**. Then we remove the current pixel from the selected orthogonal direction pattern.
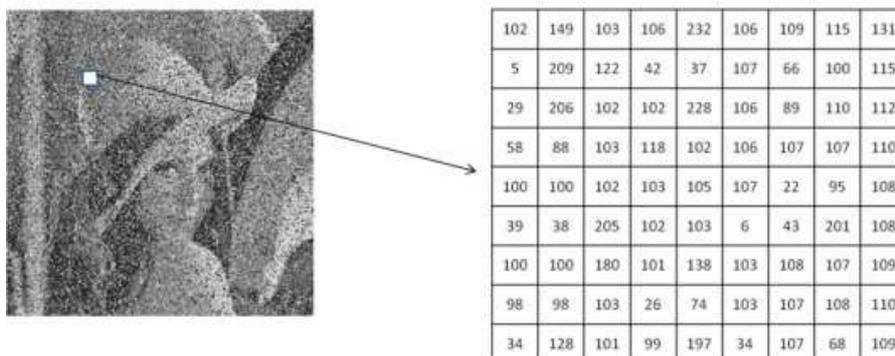
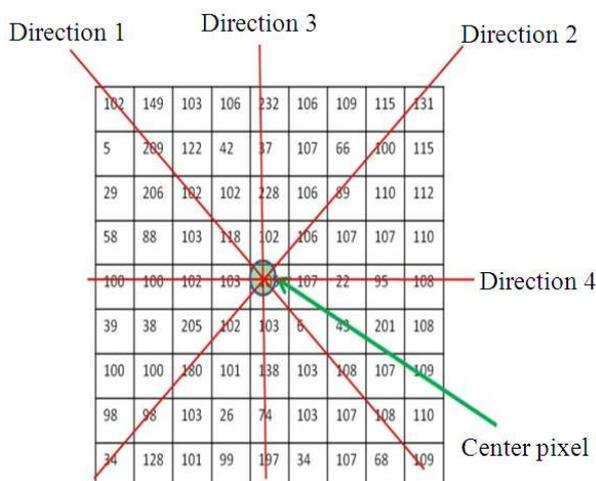**Fig. 1.** 9×9 sub-block formed from a selected sub-image

Fig. 2. 9×9 window split into 4 directions

The obtained orthogonal directional patterns are sorted in ascending order and then from these sorted values, the lowest and highest vector patterns are removed. This sorted vector contains both minimum and maximum value pixels. The vectors are found out after removing the lowest and highest elements. The Standard Deviation (SD) is calculated for each orthogonal sorted directional patterns. The minimum value of these standard deviations and its corresponding direction is considered as the optimum direction. The similarity factor between the current pixel under process and the pixels in the optimum direction is then estimated. The similarity factor is then compared with the threshold value to verify if the processed pixel is either noisy or original pixel. If it is found to be a noisy pixel, it is immediately omitted after detection and it is not carried over in further steps. Lastly the mean filter is applied over the noisy pixels.

3.2. VLSI Implementation

Figure 3 shows the block diagram of VLSI architecture for optimal detection algorithm. The architecture is comprised of five main blocks: Line buffers (odd and even), register bank, threshold block and mean filter. These blocks are explained individually in detail in the following subsections.
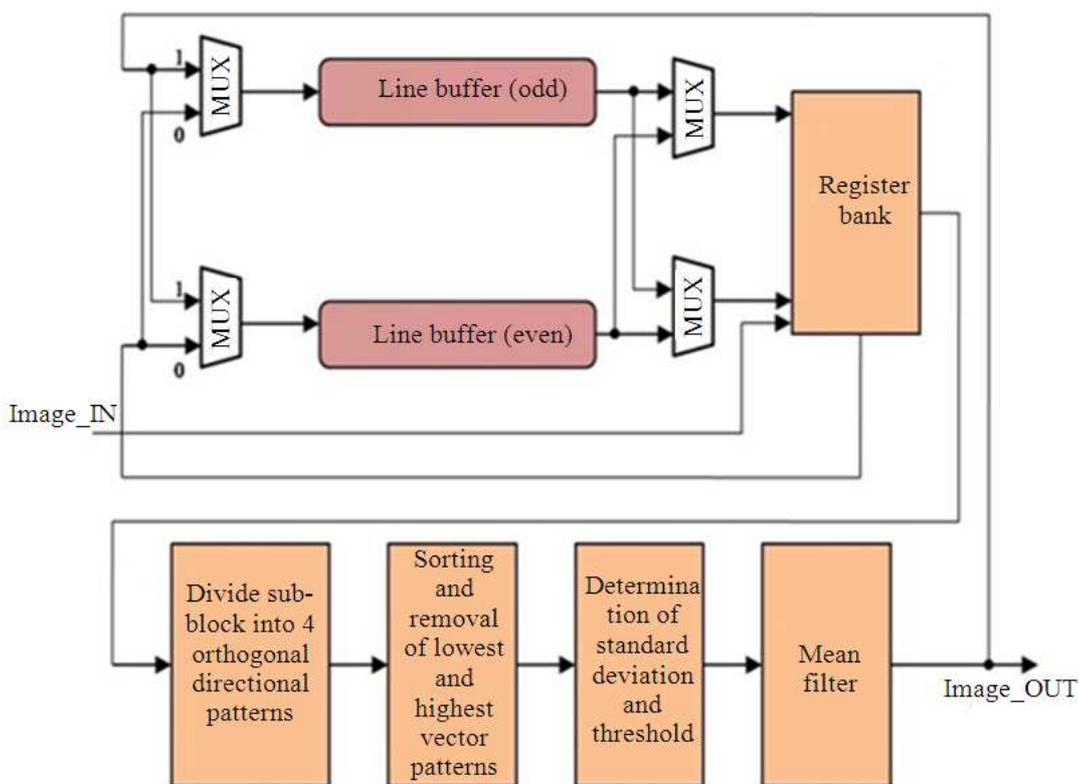
3.2.1. Line Buffer

The proposed algorithm adopts a 3×3 mask, so three scanning lines are needed. If current pixel is processed, three pixels from each row are needed to perform the denoising process. With the help of four crossover multiplexers (**Fig. 3**), three scanning lines with two line buffers are realized. Line Buffer-odd and Line Buffer-even stores the pixels at odd and even rows, respectively. In order to lower the cost and power consumed, a dual-port SRAM is used in the line buffer for read/write operation.
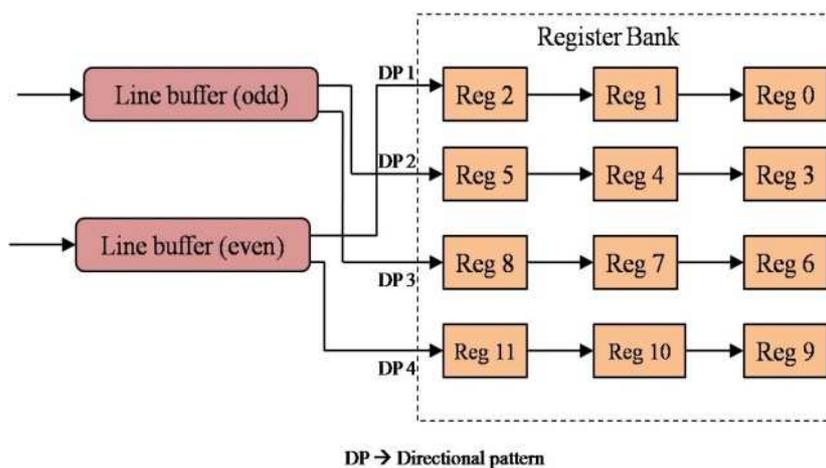
3.2.2. Register Bank

The Register Bank (RB) consists of 12 registers, Reg0-Reg11, which stores the 3×3 pixel values of the current mask. **Figure 4** shows the architecture of RB in which each 3 registers are connected serially to provide three pixel values of a row in mask and Reg4 keeps the luminance value $f_{i,j}$ of the current pixel to be denoised. The architecture of register bank is illustrated in **Fig. 4**.

3.2.3. The Mean Filter

Figure 5 shows the 2-stage pipeline architecture of the mean filter in which the |ADD| unit finds the absolute sum of two inputs. The mapping module helps in locating the four directions which are composed of noise-free pixels.

Fig. 3. Block diagram of VLSI architecture for optimal detection algorithm

DP → Directional pattern

Fig. 4. Architecture of register bank

The directional differences for the four directions are calculated. Then the smallest difference is decided by the DIV/9 unit. The last block gives the mean of the two pixel values, i.e., the filtered output.

3.2.4. Threshold Block

The architecture of the threshold block is shown in **Fig. 6**. If the pixel input value is greater than the threshold T_s, the comparator output will be logic 1 and vice-versa.
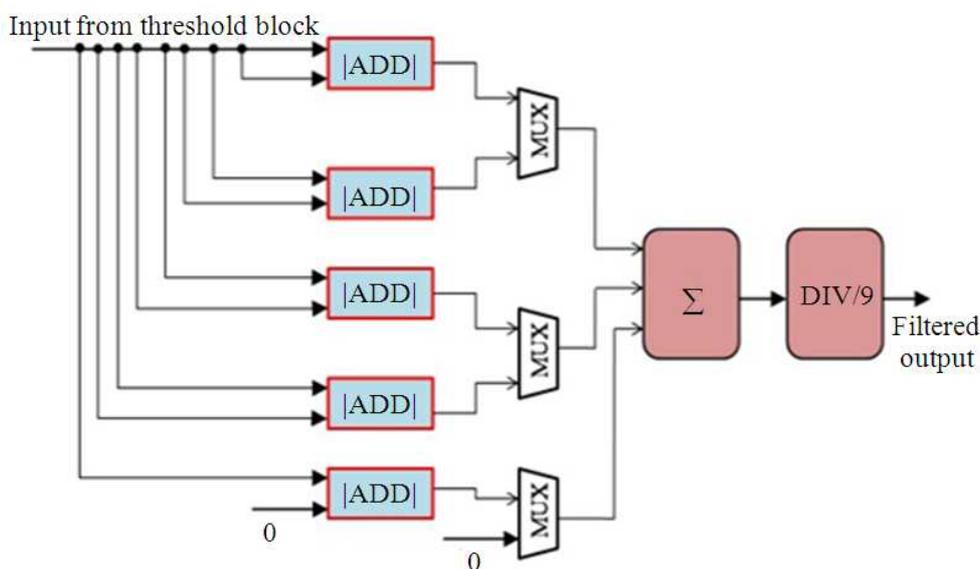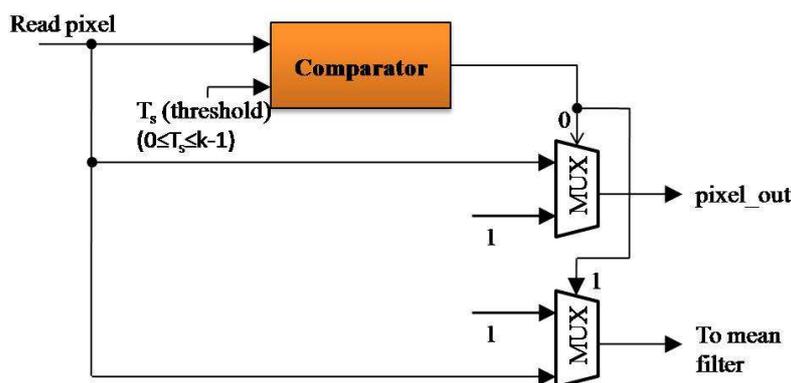
Fig. 5. Architecture of mean filter

Fig. 6. Architecture of threshold block

In our design, a single clock cycle is enough to obtain a value from one line buffer and load it into RB and the mean filter requires two clock cycles to perform the denoising processing of a pixel. The upper multiplexer outputs the pixel generated by comparator when is noise-free and another multiplexer sends the noise pixel to the mean filter for processing.
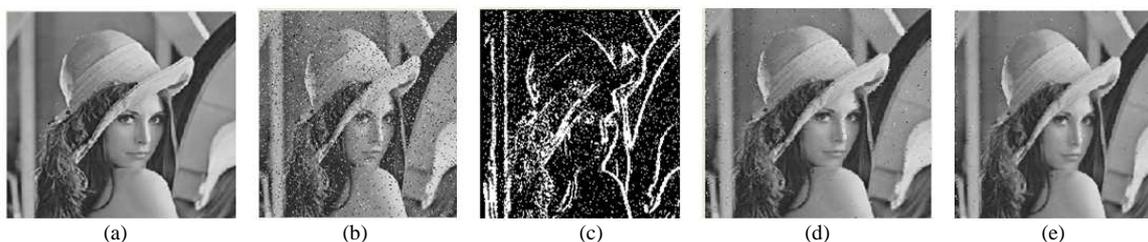
4. RESULTS

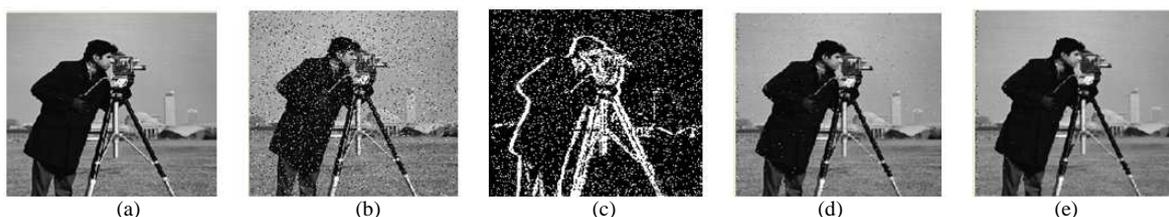### 4.1. Evaluation Details of Proposed Algorithm

To study the behavior and operational performances of different denoising techniques, various simulations were performed on the well known images: Lena, Airplane, Peppers, Boat, Gold hill and Couple. These 6 test grey-images have a size of 512×512 and resolution of 8-bits. For our experiment, we first corrupt these images by impulse noise, for example, salt-and-pepper noise. The "salt" and "pepper" noise are assumed to be equi-probable. Noise is included artificially to the original image using the MATLAB command "imnoise". The impulse noise used in our simulations are random valued and is equally spread over a range which is between [0, 255]. A window of size 9×9 has been adopted throughout the experiment.

Our proposed denoising method has a better visual quality than others and is shown in **Fig. 7 and 8**.

Fig. 7. Simulation results of Lena image, (a) Original image, (b) Noised image, (c) Noise pixels detected image, (d) Denoised image at first level and (e) Denoised image at second level
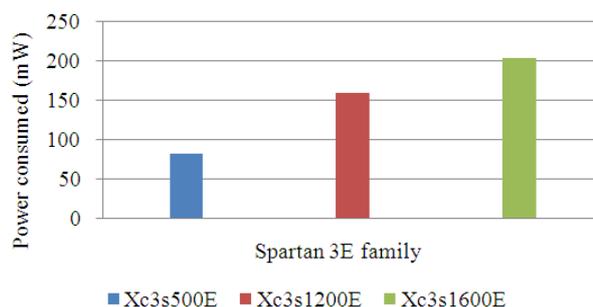

Fig. 8. Simulation results of Cameraman image, (a) Original image, (b) Noised image, (c) Noise pixels detected image, (d) Denoised image at first level and (e) Denoised image at second level

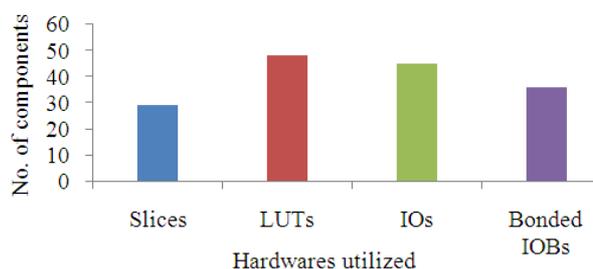## 4.2. Evaluation Details of Hardware Architecture

This proposed scheme utilized 48 LUTs and 29 slices at a maximum frequency of 200MHz. The proposed work results shows that the system incorporated with its hardware architecture leads to lower power consumption in terms of slices, Look Up Tables and Flip Flops. The various devices in the Spartan-3 family are tested against their frequency, power, quiescent current and power values and tabulated in **Table 2 and 3**. The same is also graphically plotted in **Fig. 9**. The chip summary is illustrated in **Table 4**.

The PSNR and MSE values obtained for a set of images at a noise density of 10% are tabulated and clearly shown in **Table 1**.

In the hardware evaluation section, a number of performance evaluation parameters and resource utilization parameters are being used in the design of optimal detector noise filtering algorithm. The present research is focused on the design and development of efficient hardware architecture for low power applications. The parameters considered for investigation include number of Slices (S), number of LUT's (Look up tables), Slice Latches (SL), Latches Input-Output Block (IOB) and Power Consumption (PC). The performance of the hardware utilization, i.e., the number of units of hardware used in the proposed design is tabulated in **Table 5**. The same is graphically illustrated in **Fig. 10**.

Fig. 9. Graphical illustration for power consumption

Fig. 10. Graphical plot for hardware utilities

The proposed algorithm is also compared with other existing methods in terms of gate counts and is shown in **Table 6**.

Table 1. Performance comparison of PSNR for 10% noise density

Image sequence	PSNR at level 1 denoising (dB)	PSNR at level 2 denoising (dB)	MSE at level 1 denoising (dB)	MSE at level 2 denoising (dB)
1	45.32	44.14	19.87	29.16
2	42.16	42.18	24.82	26.11
3	45.87	41.11	18.15	18.28
4	46.16	43.27	17.87	17.65
5	39.18	46.18	18.24	18.76
6	44.16	47.12	19.12	19.24
7	42.17	45.17	18.26	18.98
8	32.87	43.12	21.98	22.01
9	34.89	36.80	18.26	18.95

Table 2. Comparison of power consumptions of spartan-3 family

FPGA Family	Device specifications	Power consumption
Spartan-3E	Xc3s500E	81.37 mW
Spartan-3E	Xc3s1200E	158.95 mW
Spartan-3E	Xc3s1600E	203.27 mW

Table 3. Quiescent parameters evaluation in spartan-3E family

FPGA family	$V_{cc(int)} = 1.2V$	$V_{cc(int)} = 2.5V$
Quiescent current	69.4 mA	45 mA
Quiescent power	83.27 mW	112.5 mW

Table 4. Chip summary

Technology	90 nm spartan
Family	3E
Package	FG320
Clock frequency	200 MHz
Speed grade	- 4
Gate counts	1728

Table 5. Performance analysis of hardware utilization

Performance parameters	Proposed architecture
Slices	29
LUTs	48
IOs	45
Bonded IOBs	36

Table 6. Performance Comparison in terms of hardware utilizations

Methodology	Year	Gate Counts
Proposed	2013	1728
Lien *et al.*	2013	21k
Chen *et al.*	2010	6293

5. DISCUSSION

The proposed optimal detector noise filtering algorithm and its hardware architecture system is designed and tested on various version of Spartan-3E family device using Modelsim 6.1 and Xilinx 9.2i. To evaluate the performance of the proposed denoising technique, various simulations were performed over some of the well known images. Our proposed denoising method is quantitatively evaluated and compared in terms of subjective testing, i.e., visual quality, where recommended parameters and thresholds are used. For the quantitative testing of the reconstructed images, we make use of the Peak Signal-to-Noise Ratio (PSNR).

To prove the visual quality, the reconstructed image of proposed method is compared with that of images obtained by other denoising methods employing "Lena" and "Cameraman" images which are 60% corrupted. It has been proven that the denoised image obtained by the proposed method has a better visual quality than others and has been shown in **Fig. 7 and 8**. From the results, it is observed that our proposed denoising methodology performs very well, even at high noise ratio of 90%.

6. CONCLUSION

In this study, an optimal detector noise filtering algorithm and its efficient hardware architecture is proposed which detects and removes the impulse noise from the noise affected images. Their performances are analyzed in terms of PSNR and MSE to prove its suitability for real time image denoising. The hardware architecture for an impulse noise detection algorithm is also presented in this study to analyze its hardware utilization and power consumption. The main limitation of the research in this study is that the proposed algorithm and architecture provided best results for images only, not suitable for real time videos. Hence, this study can be extended for real time videos in future research prospects.

7. REFERENCES

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