American Journal of Applied Sciences 9 (3): 300-308, 2012
ISSN 1546-9239

Exploring Optimal Topology and Routing Algorithm for 3D Network on Chip

[1]Viswanathan, N., [2]K. Paramasivam and [3]K. Somasundaram
[1]Department of ECE, Mahendra Engineering College, Namakkal-637 503, India
[2]Department of ECE,
Bannari Amman Institute of Technology, Sathyamangalam-638 401, India
[3]Department of Mathematics,
Amrita Vishwa Vidyapeetham, Coimbatore-641 112, India

Abstract: Problem statement: Network on Chip (NoC) is an appropriate candidate to implement interconnections in SoCs. Increase in number of IP blocks in 2D NoC will lead to increase in chip area, global interconnect, length of the communication channel, number of hops transversed by a packet, latency and difficulty in clock distribution. 3D NoC is evolved to overcome the drawbacks of 2D NoC. Topology, switching mechanism and routing algorithm are major area of 3D NoC research. In this study, three topologies (3D-MT, 3D-ST and 3D-RNT) and routing algorithm for 3D NoC are presented. **Approach:** Experiment is conducted to evaluate the performance of the topologies and routing algorithm. Evaluation parameters are latency, probability and network diameter and energy dissipation. **Results:** It is demonstrated by a comparison of experimental results analysis that 3D-RNT is a suitable candidate for 3D NoC topology. **Conclusion:** The performance of the topologies and routing algorithm for 3D NoC is analysed. 3D-MT is not a suitable candidate for 3D NoC, 3D-ST is a suitable candidate provided interlayer communications are frequent and 3D-RNT is a suitable candidate as interlayer communications are limited.

Key words: SoC, 3D NoC, 3D topology, TSVs, IP blocks, traffic rate, buffer size, network diameter

INTRODUCTION

According to Moore's law, number of transistors per chip is doubled every two years that enables Integrated Circuit (IC) manufactures to provide more powerful electronic gadgets that derive multiple applications. Starting with 0.25 μm CMOS technology, wire delay dominates gate delay and the gap between wire delay and gate delay becomes wider as process technology improves, thus wires, not transistors are determining the performance of chips. Increase in number of transistors in a chip permits chip designers to integrate various components of an electronic system on a single IC to implement a complete System on a Chip (SoC) in which various components are named as cores or Intellectual Property (IP) blocks which include microprocessor, DSP, memory unit, I/O controller, analog signal or Radio Frequency module (Helali *et al*., 2006).

The constraints like very short time to test, exploit reuse and market, force the designers to design SoCs with IP blocks which are designed by different IP vendors. Major challenge in SoC is interconnecting more number of IP blocks. Nowadays, on chip communications in SoCs are realized by direct cross bar interconnections and shared buses that are inefficient on performance, cost and reliability.

Network-on-Chip (NoC) inter connection scheme is proposed as a unified solution for the design problems faced in SoC. NoC is an on-chip communication methodology proposed to resolve the increased interconnection problems in SoC. In NoC paradigm, IP blocks are connected to a packet switched network through routers, in turn routers are interconnected each other to accomplish on chip communications (Helali *et al*., 2006; Dally and Towles, 2001). NoC applies packet switching network theories to on-chip communications. A node in NoC comprises of an IP block and a router.

Advantages of NoC over conventional crossbar interconnections and shared buses (Owens *et al*., 2007):

- Wire segmentation and wire sharing design techniques are used to resolve the performance bottleneck caused by wire delay
- It uses a distributed control mechanism, resulting in a scalable interconnection network architecture

Corresponding Author: Viswanathan, N., Department of ECE, Mahendra Engineering College, Namakkal-637 503, India

- Flexible and user-defined network topology
- Point-to-point connections and a Globally Asynchronous Locally Synchronous (GALS) implementation decouple the IP blocks
- Creating derivative products by easily adding and removing IP blocks from network

Research in 3D NoC is now emerging to realize on chip communications in 3D ICs. 3D integration is achieved by stacking a number of 2D layers. Interconnection of two neighboring 2D layers is accomplished using Through-Silicon-Vias (TSVs) which provide vertical channel through vertical interconnect links (Loi *et al*., 2007).

This way, everything remains in 2D, except for the vertical links. These links can be integrated in the communication system by so-called 3D or vertical routers. Number of TSVs in an 3D architecture should be minimized as it has alignment problem and occupies a considerable chip area (Davis *et al*., 2005). In this study, three 3D network topologies and on-demand source initiated routing algorithm are presented. Topologies and routing algorithm are evaluated using simulation tool Network Simulator-2 (NS-2). Experimental results are analyzed by a comparison of various parameters of the three topologies.

This study is organized as follows: 3D NoC and its advantages, the proposed topologies and routing algorithm, materials and method, evaluation metrics, discussion and conclusion.

3D NoC: It is challenging to design mixed signal chips which combine analog processing IP blocks, such as antenna or pixel arrays, with digital IP blocks, such as microprocessors and memories, in conventional planar chip-making processes. To overcome the challenge, analog IP blocks are kept on one layer, the digital IP blocks are placed on one or two other layers and combine them in a chip which is termed as 3-D IC (Bernstein *et al*., 2007; Topol *et al*., 2006).

Advantages of 3D ICs

Chip area: Minimization of chip area is important as the yield is in general increased. Not all circuits that are manufactured function properly. The yield is the percentage of correct circuits. Causes of failure, like crystal defects, defects in the masks, defects due to contact with dust particles are less likely to affect a chip when its area is smaller.

The major advantage of 3-D IC is considerable reduction in chip length, resulting in a decrease in the chip area.

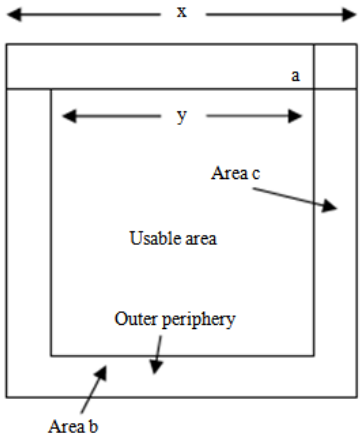

Fig. 1: 2D single layer chip area

Total chip area = x^2 and network area = y^2, where x-chip length, y-network length. It is assumed that length x of 2D chip is 68µm, y is 64 µm and length of constant a is 2 µm.

From Fig. 1, the following equations can be derived:

$$\text{Area } b = x(x-y/2) \quad (1)$$

$$\text{Area } c = y\,(x-y/2) \quad (2)$$

$$\begin{aligned} P &= x^2 - y^2 = 2(b+c) \\ &= 2*x(x-y/2) + 2*y(x-y/2), \\ \text{But } a &= x - y/2 \\ P &= 2xa + 2ya \end{aligned} \quad (3)$$

$$x^2 = 2xa + 2ya + y^2 \quad (4)$$

Using Eq. 1 and 2, the area b and c can be calculated. Total outer periphery of the chip P can be calculated using Eq. 3 and 4 gives the total chip area.

In order to reduce chip area, single layer is divided into multiple layers. Both length x and y are decreased as number of layers is increased. Chip length x reduction is not 50%, but it is only 47% as length a is constant when IP blocks are placed in two layers in lieu of placing in single layer. Similarly, there is no proportionate area reduction in 3D IC when number of layers is increased. It is concluded from Fig. 2 that length x is decreased as number of layers is increased. Trade off must be made between number of layers and chip area reduction in 3D IC as there is no proportionate reduction in length x.

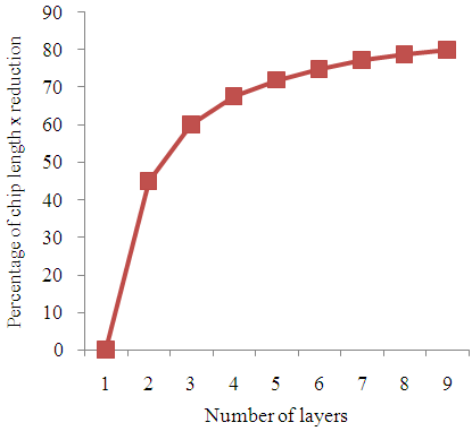

Fig. 2: Chip length x reduction

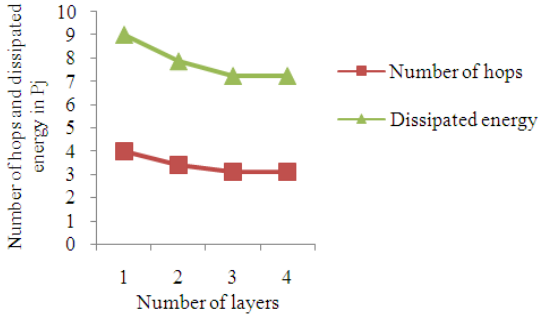

Fig. 3: Number of hops and dissipated energy in 3D IC at different number of layers

Hop count: Pavlidis and Friedman (2007) have shown that average number of hops a packet transverses from source to destination node in 3D IC is:

$$\text{Hops} = \frac{n_1 n_2 n_3 (n_1 + n_2 + n_3) - n_1 n_2}{3(n_1 n_2 n_3 - 1)} \quad (5)$$

where, $n_1 \times n_2$ is dimension of a layer and n_3 is number of layer. Multiplication of n_1 and n_2 gives number of nodes in a layer. Figure 3 shows that number of hops a packet transverses to reach destination from source node reduces when number of layers is increased

Energy dissipation: In the NoC paradigm, energy dissipation for interconnection of IP blocks depends on two independent parameters (Kahng *et al*., 2009):

- Injected traffic load
- Energy dissipated in the switches and interswitch wire segments

Energy dissipation in switches and interswitch wire segments is considered here (Banerjee *et al*., 2004).

The following assumptions are made

- Uniform traffic patterns are used for message
- Length of wire segment between two switches is fixed
- Each switch consumes 1 Pico-joule (Pj) energy to process a packet
- Each interconnect wire segment consumes 1 Pico-joule (Pj) energy to transfer a packet

Energy dissipated by a packet for 1 hop:

$$E_{packet} = \sum_{1}^{n} E_{switch} + \sum_{1}^{n-1} E_{wiresegment} \quad (6)$$

Where $E_{switch} = E_{wiresegment} + 1$

$$E_{Packet} = (2 \times D) + 1 \quad (7)$$

where, D is distance between source and designation node which is expressed in terms of hops:

$$\text{For n packets}, E_{packets} = \sum_{i=1}^{n} (2 \times D) + 1 \quad (8)$$

where, total energy consumed to transverse a packet from source to destination node is represented by E_{Packet}. E_{switch} represents the energy consumed by both buffering and switching activities of a router and $E_{wiresegment}$ represents the energy consumed by charging and discharging of link capacitance. Each packet transverses (n+1) switches through n wire segments, thus hop count is n.

It is considered that number of IP blocks to be placed is 36 and maximum number of layers is 4. Energy dessipation for single packet is expressed in Eq. 6. Energy dissipation can also be expressed using Eq. 7 and total energy dessipated for n packets can be computed using Eq. 8. Average number of hops for a packet is calculated using Eq. 5 from which average energy dissipation is computed using Eq. 7. From Fig. 3, it is concluded that average energy dissipation is reduced as number of layers is increased.

In addition to chip area, hop count and energy dissipation, 3-D ICs have following advantages:

- Layer yield decreases exponentially with increases in layer size, so splitting a single layer design into two or more can save money in the end
- Increasing the number of transistors that are within one clock cycle of each other

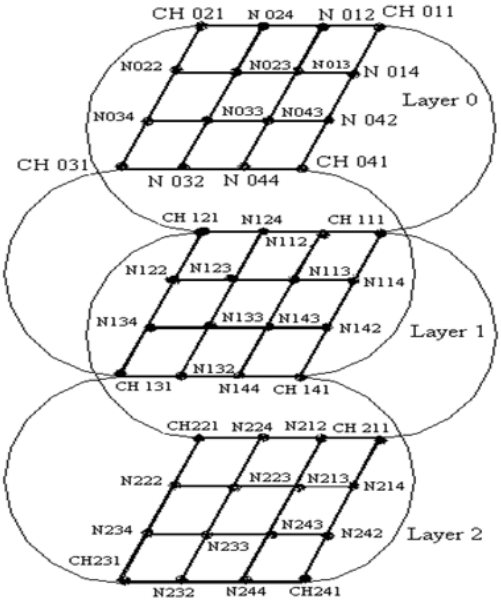

Fig. 4: 3D-Mesh Topology (3D-MT)

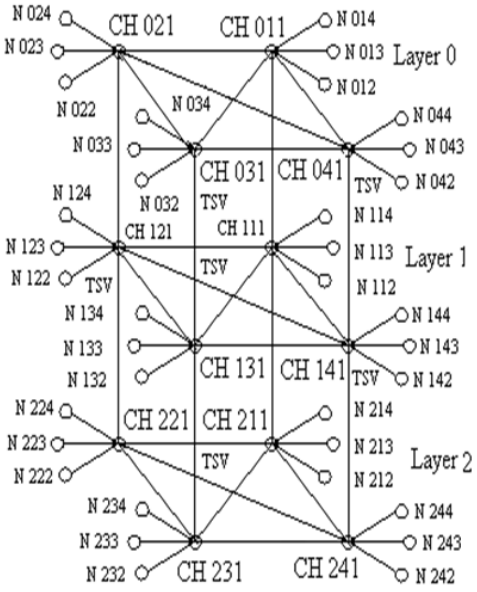

Fig. 5: 3D-Star Topology (3D-ST)

- Maximum global-interconnect length and the average global-interconnect length both decrease by a factor equal to the square root of the number of layers being stacked
- Higher packing density

3D NoC is becoming an emerging research area as 3D ICs apply NoC to realize on chip communications.

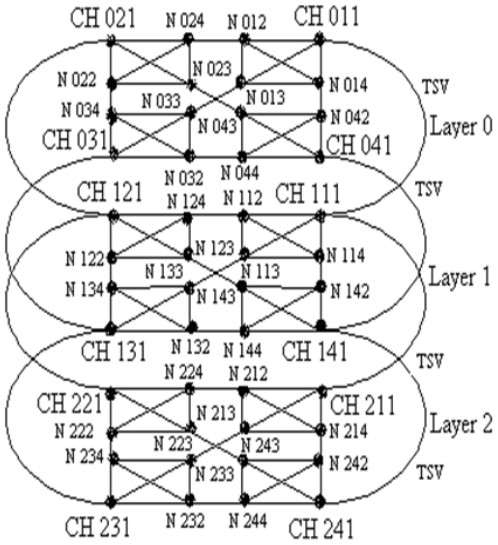

Fig. 6: 3D-Recursive Network Topology (3D-RNT)

Topologies and routing algorithm: Mesh, Star and WK recursive network topologies are very familiar topologies in 2D NoC. Three 3D topologies, Mesh Topology (3D-MT), Star Topology (3D-ST) and Recursive Network Topology (3D-RNT) are derived by modifying the 2D topologies and presented here as shown in Fig. 4-6. Three layers are considered in each topology in which IP blocks may be either homogeneous or heterogeneous as the topologies have more than one layer. In the topologies, cluster is formed by grouping four nodes with one node is identified as Cluster Head (CH) which can act as CH as well as node. A layer has four clusters, thus total number of nodes in a layer is sixteen (Feero and Pande, 2009; Loh, 2008).

IP blocks are connected to routers, in turn routers are interconnected using horizontal interconnect links. Vertical interconnect links (TSVs) are used to interconnect neighboring layer routers to form 3D network. Interlayer communications are realized only through CHs. CHs and other nodes can be identified by an ID of three digits XYZ. First digit X of the ID represents a layer, second digit Y represents a cluster and third digit Z represents either a node or CH. In 3D-ST, CHs in a layer are interconnected to communicate each other in single hop.

Intercluster nodes cannot communicate each other, they will communicate each other only through CHs. In 3D MT and 3D-RNT, CHs will communicate each other only through intercluster nodes that are allowed to communicate each other in single hop.

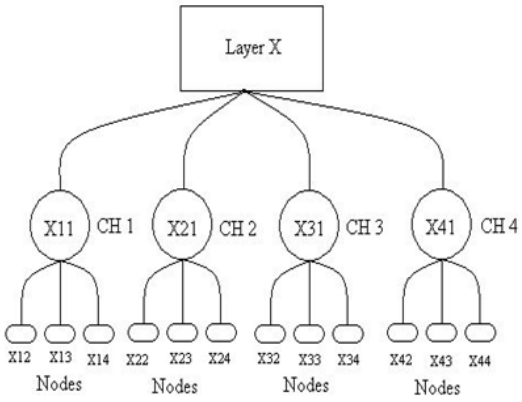

Fig. 7: Tree representation of the topologies

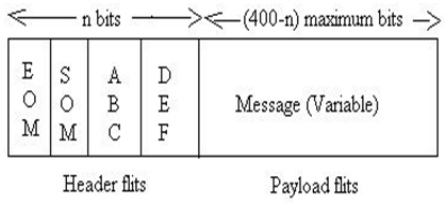

Fig. 8: Packet format

For 3D-ST, hierarchical shortest path is established between source node of ID 242 and destination node of ID 032.

Source node ID → 242→ layer 2, cluster 4, node 2

241→ layer 2, cluster 4, node 1
141→ layer1, cluster 4, node 1
041→ layer 0, cluster 4, node 1
031→ layer 0, cluster 3, node 1
032→ layer 0, cluster 3, node 2
Destination node ID:032

Shortest path between nodes of ID 242 and 032 in 3D- MT and 3D-RNT is
242→241→141→041→044→032

Hierarchy and clustering are two efficient network techniques as they provide scalability, higher performance, easy maintainability, manageability and resource reusability, are applied in developing 3D routing algorithm. Routing is an on demand and source initiating. Hierarchy and clustering of nodes are represented using tree structure as shown in Fig. 7. The tree has three levels in its hierarchy, level 1 represents layer, level 2 represents CHs and level 3 represents nodes. A CH and nodes connected to the CH will form a cluster.

Figure 8 shows packet format used to transfer message in the 3D network. The header flits have n bits in which first bit is End of Message (EOM) and the second bit is Start of Message (SOM). The rest of the bits (n-2) indicates ID of the source and destination nodes. Payload flits contain variable length message of maximum length 400-n bits as packet size is 50 bytes.

Pseudo code for routing algorithm for 3D-ST:

```
// Declare source node ID as ABC and destination
   node ID  DEF
// Declare Layer ID as 0, 1 and  2
// Hierarchical level-1→ Reaching destination
   layer
// Level-2→ Reaching destination CH
// Level-3→ Reaching destination node which may
   be either a CH or node
// Route packet to hierarchical level-1
If packet source ID first digit A = = Current layer
ID,
 Deliver packet in current layer
   Else if A < D
    Route packet to Down layer
     Else
      Route packet to Up layer
       // Route packet to level-2
          Else if E>=1
          Route packet to CH E
            // Route packet to level-3
              Else if F = = 1
                Deliver packet to E^th CH
                  Else if F >1
                    Deliver packet to F^th node in
                     the E^th cluster
                  End if
              End if
          End if
 End if
```

Pseudo code for routing algorithm for 3D-MT and 3D-RNT

```
// Declare source node ID as ABC and destination
   node ID  DEF
// Declare Layer ID as 0, 1 and 2
// Hierarchical level-1→ Reaching destination
   layer
// Level-2→ Reaching destination Cluster
// Level-3→ Reaching destination node which
   may  be a CH or node
// Route packet to hierarchical level-1
If packet source ID first digit A = = Current layer
ID,
 Deliver packet in current layer
    Else if A < D
```

```
Route packet to Down layer
  Else
    Route packet to Up layer
      // Route packet to level-2
        Else if E>=1
          Route packet to cluster E
            // Route packet to level-3
              Else if F = = 1
                Deliver packet to E^th CH
                  Else if F >1
                    Deliver packet to F^th node in
                     the E^th cluster
                  End if
              End if
        End if
End if
```

MATERIALS AND METHODS

3D Network topologies and routing algorithm are evaluated using Network Simulator-2 (NS-2), an open source simulator tool which runs in Linux environment on Intel Pentium IV, 2.4 GHz processor with 1GB memory. Various input parameters used in the simulation are listed in Table 1. Modified OSI model is exploited in NS-2 as five layers are required to define communication protocols between IPs in NoC. Five traffic source-sink pairs are selected randomly and are concurrently active.

Simulation output results are observed for latency at two cases:

- Different switch buffer size at fixed injected load
- Different traffic rate at fixed switch buffer size

Two different traffic rates, 4.5 Kbps and 1 Kbps are assigned at each traffic. Number of packets sent by individual source is 563 at the rate 4.5 Kbps and 126 at the rate 1 Kbps respectively. Table 2 shows simulation results for latency at the traffic rate 4.5 Kbps with switch buffer size varies from 5-50 packets.

Switch buffer size is fixed as 50 packets and packets are injected into the network at different traffic rates. Simulation results for latency are shown in Table 3.

Evaluation metrics: Following evaluation parameters are selected for performance evaluation of the topologies and routing algorithm:

- Latency
- Drop probability

Table 1: NoC and NS-2 Parameters Mapping

NoC parameters	Mapping of NS-2 constraints
Connection	Router to router
Transmission Protocol	UDP
Router buffer size	Maximum 50 packets
Packet size	50 bytes
Router queue mechanism	Drop tail
Routing strategy	Dynamic
Routing Protocol	Hierarchical and shortest path
Duplex band width	5Kb
Connection time	50 sec
Simulation time	100 sec
Traffic behavior	CBR
Traffic generator	exponential

Table 2: Simulation results at traffic rate 4.5 Kbps

	Latency in seconds		
Switch buffer size	3D-MT	3D-ST	3D-RNT
5	0.57428	0.54695	0.51962
10	0.82539	0.79805	0.77072
15	1.06706	1.03973	1.01239
20	1.30103	1.27369	1.24636
25	1.52831	1.50097	1.47364
30	1.74969	1.70093	1.69503
35	1.96605	1.93871	1.91138
40	2.17789	2.15043	2.12309
45	2.38538	2.35804	2.33071
50	2.58933	2.56199	2.53467

Table 3: Simulation results at fixed switch buffer size

	Latency in seconds		
Traffic rate (Kbps)	3D-MT	3D-ST	3D-RNT
0.5	0.38266	0.35533	0.32800
1	0.38266	0.35533	0.32799
1.5	0.38266	0.35533	0.32799
2	0.38266	0.35533	0.32800
2.5	0.38333	0.35599	0.32866
3	2.39848	2.37115	2.34381
3.5	2.61101	2.58368	2.34381
4	2.64230	2.61496	2.58633
4.5	2.58933	2.56233	2.53539
5	2.26576	2.23843	2.23466
5.5	3.82345	3.86342	3.83618
6	4.40963	4.38229	4.35496

- Network Diameter
- Energy Dissipation

RESULTS AND DISCUSSION

Latency: Latency is defined as the time taken by a packet to go through a communication path from its source to its intended sink.

Latency is calculated in two cases:

- For different switch buffer size at the fixed traffic rate 4.5 and 1 Kbps
- For different traffic rate at fixed switch buffer size of 50 packets

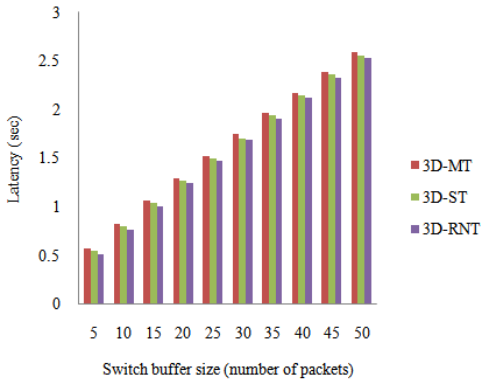

Fig. 9: Latency at the traffic rate 4.5Kbps

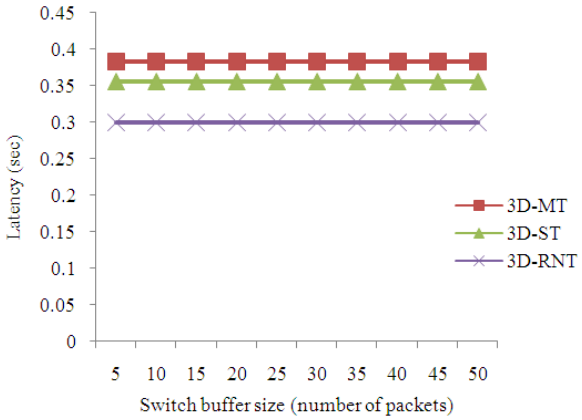

Fig. 10: Latency at the traffic rate 1 Kbps

Packets wait more time in switch buffer as number of packets increases, thus latency of a packet is increased. On comparing with 3D-MT and 3D-ST, latency is decreased in the 3D-RNT as shown in Fig. 9 at the traffic rate 4.5 Kbps as the topology has lesser number of links between the five randomly chosen source-sink pairs.

For the three topologies, it is observed from Fig. 10 that latency remains constant when buffer size increases at the traffic rate 1 Kbps which indicates that switch buffer size is not sensitive to the communication load at 1 Kbps. Performance of 3D-RNT is superior to other topologies with respect to latency at the traffic rate 1 Kbps.

When traffic rate exceeds 2.5 Kbps, there is rapid change in latency as shown in Fig. 11. Switches utilize their buffer capacity to maximum possible extent so as to avoid packet drop up to traffic rate around 2.5 Kbps. Packet drop starts as traffic rate exceeds around 2.5 Kbps owing to the shortage of switch buffer capacity.

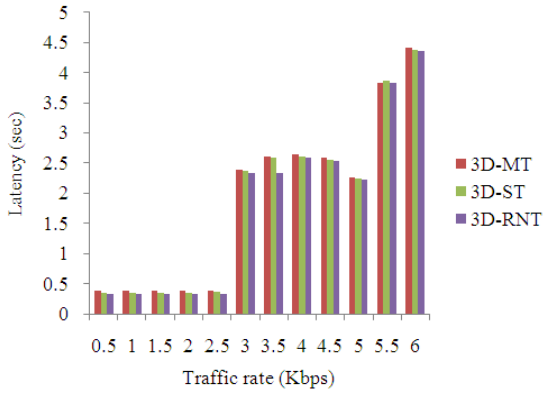

Fig. 11: Latency at fixed switch buffer size

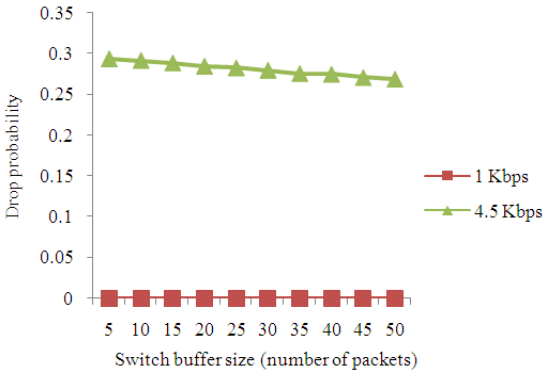

Fig. 12: Drop probability at traffic rate 4.5 and 1 Kbps

It is concluded that the performance of 3D-RNT with respect to latency is superior to 3D-MT and 3D-ST at any injected traffic rate and switch buffer size.

Drop probability: Drop probability is calculated from the number of packets sent by the source and received by the sink.

It is also calculated for the two cases.

Case I: Performance of the three topologies is identical with respect to drop probability as same number of packets is received in the three topologies at all instances. It is observed from Fig. 12 that drop probability is insensitive with respect to switch buffer size at traffic rate 1 Kbps.

Case II: Behavior of the three topologies is identical. For the three topologies, drop probability is zero up to the injected traffic rate 2.5Kbps. Figure 13 shows that performance of the topologies starts degraded when traffic rate exceeds 2.5Kbps as packet drops start around 2.5 Kbps.

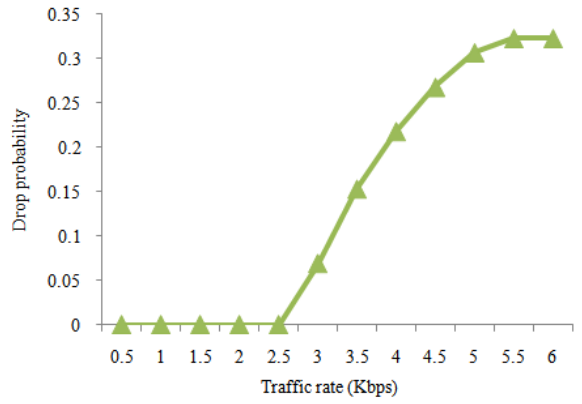

Fig. 13: Drop probability at fixed switch buffer size

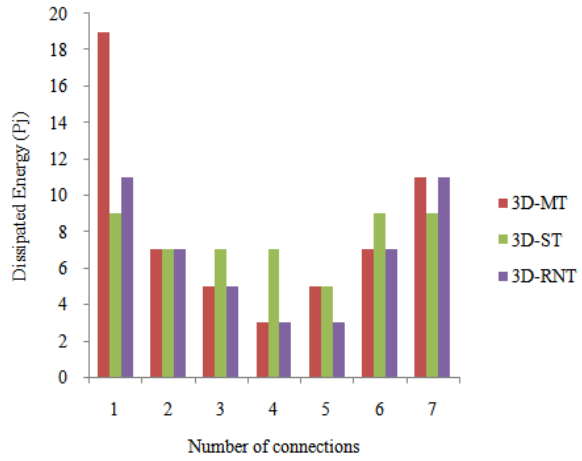

Fig. 14: Energy dissipated to transfer a packet

Network diameter: An important parameter of any hierarchical network topology is network diameter which can be defined as the maximum internodes distance i.e. it is the maximum number of links that must be transversed to send a packet to any node along a shortest path. Time for sending a packet from one node to farthest away node in a network can be reduced as the network diameter is lower. Typically, to improve the performance and speed of network transmission, it needs to reduce the network diameter.

To find total distance d of a network, one node is taken as source node and its distances to other nodes are calculated and finally number of nodes is multiplied by number of hops. Node 021 is assumed as source node and distance to all other nodes from the source node is given in Table 4 (Daneshtalab *et al*., 2009; Xu *et al*., 2009):

- For 3D-MT, distance
  d =1 ×3+2×6+3×8+4×9+5×9+6×7+7×4+8×1 = 198

Table 4: Distance from one node to others

Nodes from which distance equals	Number of nodes		
	3D-MT	3D-ST	3D-RNT
1	3	7	4
2	6	16	8
3	8	15	10
4	9	9	7
5	9	--	18
6	7	--	--
7	4	--	--
8	1	--	--

Table 5: Distance at seven source-sink pairs

Transmitting node	Receiving node	Distance (D)		
		3D-MT	3D-ST	3D-RNT
231	012	9	4	5
232	242	3	3	3
213	242	2	3	2
123	113	1	3	1
122	124	2	2	1
141	032	3	4	3
211	043	5	4	5

- For 3D-ST, distance
  d = 1× 7 + 2 × 16 + 3 × 15 + 4 × 9 = 120
- For 3D-RNT,
  d = 1 × 4 + 2 × 8 + 3 × 10 + 4 × 7 + 5 × 18 =168

3D-MT is not a suitable candidate as distance d is higher than other topologies. 3D-ST is an appropriate candidate as more number of nodes having lesser distance from the source node.

It is concluded that 3D-MT is not suitable candidate as total distance d is higher than other two topologies diatance. 3D-ST is a suitable candidate provided interlayer traffic is very frequent as all other nodes from the source node have distance less than 5.

Energy dissipation: Distance (D) to transfer a packet for seven randomly chosen source-sink pairs are calculated and given in Table 5. Energy dissipation to transfer a single and multiple packets can be calculated using (Eq.7 and 8) respectively.

From Fig. 14, it is concluded that 3D-ST dissipates lesser energy when traffic is in interlayer. In intralayer communications, both 3D-MT and 3D-RNT dissipates lesser energy.

CONCLUSION

In this study, three 3D topologies and hierarchical, cluster based routing algorithm for 3D NoC are presented. Simulation results for the performance of the three topologies are analyzed by a comparison of

various parameters of the topologies. As far as drop probability is concerned, performance of the three topologies is identical as same number of packets is received at all instances. It is shown using the parameter latency that 3D-RNT is out performing than 3D-MT and 3D-ST. It is concluded that 3D-MT is not suitable candidate on comparing the performance of the three topologies in terms of latency, network diameter and energy dissipation. 3D-RNT is a suitable candidate for the applications where interlayer communications of IP blocks are very limited. 3D-ST is an appropriate topology candidate of 3D NoC for the applications where frequent interlayer communications of IP blocks are required.

REFERENCES

Banerjee, N., P. Vellank and K.S. Chatha, 2004. A power and performance model for network-on-chip architectures. Proceedings of the Design, Automation and Test in Europe Conference and Exhibition, Feb. 16-20, IEEE Xplore Press, USA., pp: 1250-1255. DOI: 10.1109/DATE.2004.1269067

Bernstein, K., P. Andry, J. Cann, P. Emma and D. Greenberg *et al*., 2007. Interconnects in the third dimension: Design challenges for 3D ICs. Proceedings of the 44th Annual Design Automation Conference, Jun. 04-08, ACM, USA., pp: 562-567. DOI: 10.1145/1278480.1278623

Dally, W.J. and B. Towles, 2001. Route packets, not wires: On-chip interconnection networks. Proceedings of the Design Automation Conference Jun. 22-22, IEEE Xplore Press, USA., pp: 684-689. DOI: 10.1109/DAC.2001.156225

Daneshtalab, M., M. Ebrahimi, S. Mahammadi and A. Afzali-Kusha, 2009. Low-distance path-based multicast routing algorithm for network-on-chips. IET Comput. Digital Techn., 3: 430-442. DOI: 10.1049/iet-cdt.2008.0086

Davis, W.R., J. Wilson, S. Mick, J. Xu and H. Hua *et al*., 2005. Demystifying 3D ICS: The pros and cons of going vertical. IEEE Design Test Comput., 22: 498-510. DOI: 10.1109/MDT.2005.136

Feero, B.S. and P.P. Pande, 2009. Networks-on-chip in a three-dimensional environment: A performance evaluation. IEEE Trans. Comput., 58: 32-45. DOI: 10.1109/TC.2008.142

Helali, A., A. Soudani, J. Bhar and S. Nasri, 2006. Study of network on chip resources allocation for QoS management. J. Comput. Sci., 2: 770-774. DOI:10.3844/Jcssp.2006.770.774

Kahng, A.B., B. Li, L.S. Peh and K. Samadi, 2009. Orion 2.0: A fast and accurate NoC power and area model for early-stage design space exploration. Proceedings of the Conference on Design, Automation and Test in Europe, Apr. 20-24, ACM, Nice, France, pp: 423-428.

Loh, G.H., 2008. 3D-stacked memory architectures for multi-core processors. Proceedings of the 35th International Symposium on Computer Architecture, Jun. 21-25, IEEE Xplore Press, Beijing, pp: 453-464. DOI: 10.1109/ISCA.2008.15

Loi, I., F. Angiolini and L. Benini, 2007. Supporting vertical links for 3D networks-on-chip: Toward an automated design and analysis flow. Proceedings of 2nd International Conference on Nano-Networks, Sep. 24-26, ACM, Catania, Italy, pp: 1-5.

Owens, J.D., W.J. Dally, R. Ho, D.N. Jayasimha and S.W. Keckler *et al*., 2007. Research challenges for on-chip interconnection networks. IEEE Micro., 27: 96-108. DOI: 10.1109/MM.2007.4378787

Pavlidis, V.F. and E.G. Friedman, 2007. 3-D topologies for networks-on-chip. IEEE Trans. Very Large Scale Integrat. Syst., 15: 1081-1090. DOI: 10.1109/TVLSI.2007.893649

Topol, A.W., D.C.L. Tulipe, L. Shi, D.J. Frank and K. Bernstein *et al*., 2006. Three-dimensional integrated circuits. IBM J. Res. Dev., 50: 491-506. DOI: 10.1147/rd.504.0491

Xu, Y., Y. Du, B. Zhao, X. Zhou and Y. Zhang, 2009. A low-radix and low-diameter 3D interconnection network design. IEEE 15th International Symposium on High Performance Computer Architecture, Feb. 14-18, IEEE Xplore Press, Raleigh, NC, pp: 30-42. DOI: 10.1109/HPCA.2009.4798234