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Spartan-3AN Field Programmable Gate Arrays Truncated Multipliers Delay Study

Mohammed H. Al Mijalli
Department of Biomedical Technology, College of Applied Medical Sciences,
King Saud University, Riyadh, Saudi Arabia

Abstract: Problem statement: The image processing applications, such as MPEG video compression used in CT scan frames requires real time conditions and the algorithms should be verified and optimized before implementation which cannot be done with Application Specific Integrated Circuits (ASICs) because they are not reconfigurable and cost is very high. **Approach:** The FPGA is a viable technology that could be implemented and reconfigured at the same time, since FPGA have the benefit of hardware speed and the flexibility of software. **Results:** The results obtained from Sparatn-3An FPGA show that the mean delay time for four multipliers, clearly indicates as the size of multiplier increases the mean delay time also increases. **Conclusion:** The FPGA based truncated multipliers could also be used in medical imaging technology.

Key words: Field Programmable Gate Array (FPGA), spartan-3AN, Digital Signal Processing (DSP), Application Specific Integrated Circuits (ASICs), xilinx family

INTRODUCTION

Digital Signal Processing (DSP) in fact requires intensive scientific computations for real time imaging processes. The multipliers play a crucial role in such delicates and important computations. In DSP, General Purpose Signal Processing (GPSP) and application specific architecture for DSP the computational complexity of algorithms has increased to such extent that they require fast and efficient parallel multipliers.

Implementation of DSP algorithm demands using Application Specific Integrated Circuits (ASICs). The costs for ASICs are high; on top of that the algorithms should be verified and optimized before implementation. The Field Programmable Gate Arrays (FPGAs) have emerged as a platform of choice for efficient hardware implementation of computation intensive algorithms. FPGA have the benefit of hardware speed and the flexibility of software. The three main factors that play an important role in FPGA based design are the targeted FPGA architecture, Electronic Design Automation (EDA) tools and design techniques employed at the algorithmic level using hardware description languages. In FPGAs, the choice of the optimum multiplier involves three key factors: area, propagation delay and reconfiguration time.

Truncated multipliers do not form all of the least-significant columns in the partial-product matrix as more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced and in many cases the delay also decreases (Rais, 2009a).

To date, many research efforts have been presented in literature to achieve hardware efficient implementation of a truncated multiplier (Rais, 2009a; 2009b; Rais, 2010a). In this study, a hardware design and implementation of FPGA based parallel architecture for standard and truncated multipliers is presented. The truncated multiplier has shown much more reduction in device utilization as compared to standard multiplier. The basic idea of these techniques is to discard some of the less significant partial products and to introduce a compensation circuit that partly compensates for the dropped terms, thereby reducing approximation error. Truncated multiplication provides an efficient method for reducing the power dissipation and area of rounded parallel multiplier (Rais, 2010b). In this study, analysis of variance study of delay in truncated multipliers is presented.

MATERIALS AND METHODS

Architecture platform: Due to the parallel nature, high frequency and high density of modern FPGAs, they make an ideal platform for the implementation of computationally intensive and massively parallel architecture. A brief introduction about Spartan-3 FPGAs from Xilinx is presented.

Spartan-3 FPGAs: The Spartan-3 FPGA belongs to the fifth generation Xilinx family. It is specifically designed to meet the needs of high volume, low unit

cost electronic systems. The family consists of eight member offering densities ranging from 50,000 to five million system gates (Xilinx, 2008) The Spartan-3 FPGA consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, dedicated multipliers (18×18) and digital clock managers (DCMs), Spartan-3 family includes Spartan-3L, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs. Particularly, the Spartan-3AN is used as a target technology in this study. Spartan-3AN combines all the feature of Spartan-3A FPGA family plus leading technology in-system flash memory for configuration and nonvolatile data storage.

RESULTS

FPGA design and implementation and one way ANOVA statistics: The design of standard and truncated 4×4, 6×6, 8×8 and 12×12-bit multipliers are done using and implemented in a Xilinx Spartan-3AN XC3S700AN (package: fgg484, speed grade: -5) FPGA using the Xilinx ISE 9.2i design tool. A one-way ANOVA is applied to find out the effect of different multipliers on the mean delay time for Spartan-3AN device.

DISCUSSION

Table 1 summarizes the FPGA device resources utilization for standard and truncated 4×4, 6×6, 8×8 and 12×12-bit multipliers. FPGA layouts of the standard 4×4, 6×6, 8×8 and 12×12-bit multipliers are shown in Figs. 1-4. FPGA layouts of truncated 4×4, 6×6, 8×8 and 12×12-bit multipliers are shown in Figs. 5-8.

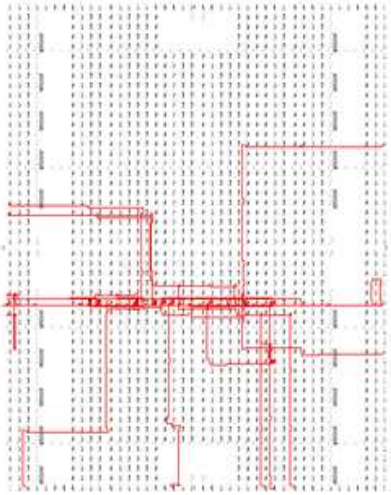

Fig. 1: FPGA layout of standard 4×4-bit multiplier

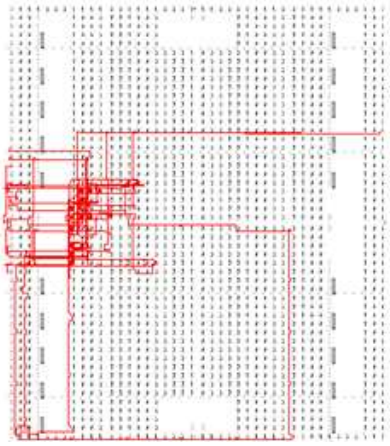

Fig. 2: FPGA layout of standard 6×6-bit multiplier

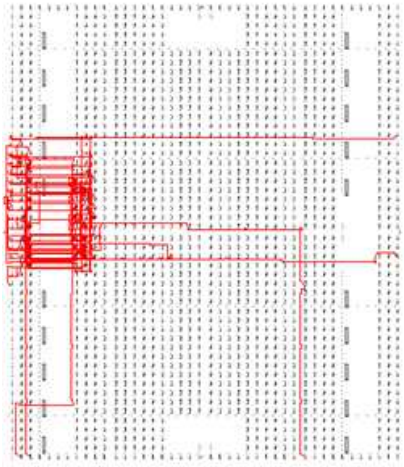

Fig. 3: FPGA layout of standard 8×8-bit multiplier

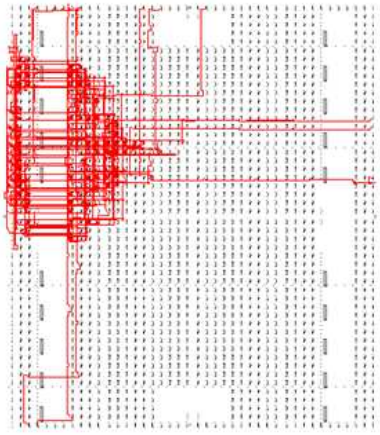

Fig. 4: FPGA layout of standard 12×12-bit multiplier

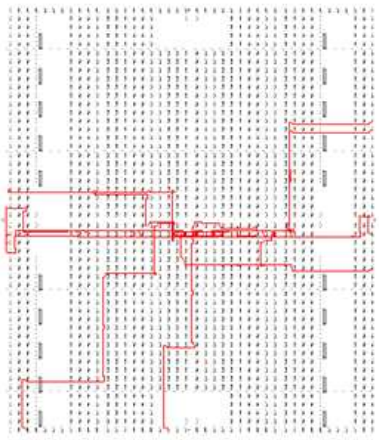

Fig. 5: FPGA layout of truncated 4×4-bit multiplier

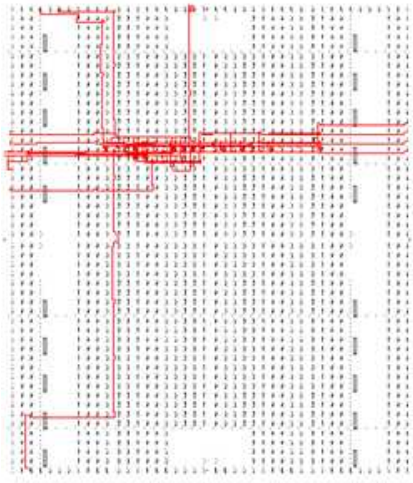

Fig. 6: FPGA layout of truncated 6×6-bit multiplier

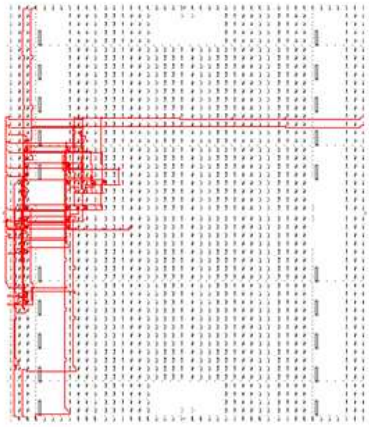

Fig. 7: FPGA layout of truncated 8×8-bit multiplier

Fig. 8: FPGA layout of truncated 12×12-bit multiplier

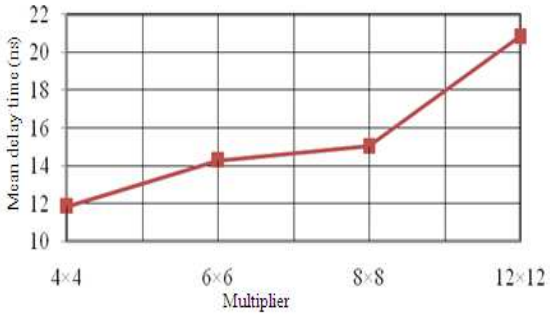

Fig. 9: Mean delay time for the four multipliers

Table 2 shows the one-way ANOVA on Spartan-3AN FPGA device. The multipliers 4×4, 6×6, 8×8 and 12×12 are used for this analysis. The statistical analysis is done by using SPSS program. There is a statistically significant difference at the 0.05 level in delay time for the multipliers [F(3, 16) = 102.31, p = 0.000]. The mean values of delay time for the multipliers are compared by using one-way ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level.

The test indicates that the mean value of the delay time for multiplier 4×4 (Mean = 11.84, Standard Deviation = 0.72) is significantly different from multiplier 6×6 (Mean = 14.28, Standard Deviation = 0.67), multiplier 8×8 (Mean = 15.02, Standard Deviation = 0.68) and multiplier 12×12 (Mean = 20.82, Standard Deviation = 1.18). There is also significant difference between the delay time for multiplier 12×12 and the others three. However, the delay time for multiplier 6×6 does not differ significantly from multiplier 8×8. Figure 9 shows the mean delay time for the four multipliers, which clearly indicates as the size of multiplier increases the mean delay time also increases.

Table 1: FPGA resource utilization for standard and truncated multiplier for Spartan-3AN XC3S700AN (package: fgg484, speed grade:-5) (Rais, 2010a)

Bit Width	Multipliers	Four input LUTs (11776)	Occupied slices (5888)	Bonded IOBs (372)	Total equivalent gate count	Average connection delay (ns)	Maximum pin delay (ns)
4×4	Standard	30	16	16	180	1.421	3.598
	Truncated	18	11	12	111	1.272	2.705
6 ×6	Standard	67	36	24	402	1.238	4.873
	Truncated	43	24	18	261	1.096	2.722
8×8	Standard	121	62	32	726	1.085	3.968
	Truncated	76	40	24	456	1.072	3.641
12×12	Standard	289	148	48	1734	1.079	3.766
	Truncated	164	87	36	984	1.307	3.971

Table 2: Multiple comparisons of delay time (ns) for four multipliers using Tukey's HSD post-hoc test

					95% confidence interval	
(I) multipliers	(J) multipliers	Mean Difference (I-J)	Std. Error	Sig.	Lower bound	Upper bound
4×4	6×6	-2.4400*	0.5319	0.002	-3.9617	-0.9183
	8×8	-3.1800*	0.5319	0.000	-4.7017	-1.6583
	12×12	-8.98000*	0.5319	0.000	-10.5017	-7.4583
6×6	4×4	2.4400*	0.5319	0.002	0.9183	3.9617
	8×8	-0.74	0.5319	0.522	-2.2617	0.7817
	12×12	-6.5400*	0.5319	0.000	-8.0617	-5.0183
8×8	4×4	3.1800*	0.5319	0.000	1.6583	4.7017
	6×6	0.74	0.5319	0.522	-0.7817	2.2617
	12×12	-5.8000*	0.5319	0.000	-7.3217	-4.2783
12×12	4×4	8.9800*	0.5319	0.000	7.4583	10.5017
	6×6	6.5400*	0.5319	0.000	5.0183	8.0617
	8×8	5.8000*	0.5319	0.000	4.2783	7.3217

* The mean difference is significant at the .05 level

CONCLUSION

In this study we have presented hardware design and implementation of FPGA based parallel architecture for standard and truncated multipliers utilizing . The design was implemented on Xilinx Spartan-3AN XC3S700AN FPGA device using the ISE 9.2i design tool. The objective is to present a mean delay time for the four multipliers, which clearly indicates as the size of multiplier increases the mean delay time also increases.

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